

Model Name: GA-Z170X-UD3

Rev 1.0

SHEET TITLE

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU_LGA1150-A
05	CPU_LGA1150-B_DDR4
06	CPU_LGA1150-C
07	CPU_LGA1150-D
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09	DDR4 CHANNEL B 1,2
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11	PCH_DMI,USB,PCIE
12	PCH MISC
13	PCH_SATA,PCIE,SATA_EXPRESS
14	PCH_PWR,GND
15	DUAL BIOS
16	ITE 8628 LPC IO
17	HMW
18	FAN_CTRL--SIO
19	PCI EXPRESS X16 SLOT
20	PCI EXPRESS X4 SLOT(PCH)
21	PCI EXPRESS X1 SLOTS/SWITCH
22	M.2 X4
23	M.2 X4 (2nd)
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26	ISL95856 PWM
27	ISL95856 MOS_VCORE-Ferrite
28	ISL95856 MOS_VCCGT-Ferrite
29	VCCSA_VCCIO_VCCPLL
30	RT8120_DDR_CHOKE

SHEET

TITLE

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32	RT8120_PCH
33	DISCRETE POWER
34	NCT3933
35	ATX POWER , A -PROCHOT
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39	PTN3356 - DP to VGA - Conn
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44	Realtek ALC1150
45	REAR AUDIO JACK
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47	F_USB_BOX_Header
48	COM,LPT,TPM ,THB,TURBO
49	F_PANEL
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56	M.2 SWITCH
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59	ALPINE RIDGE POWER
60	NTC MAP

Gigabyte Technology

File			Cover Sheet
Size	Document Number	GA-Z170X-UD3	Rev 1.0
Custom			
Date:	Monday, July 06, 2015	Sheet	1 of 60

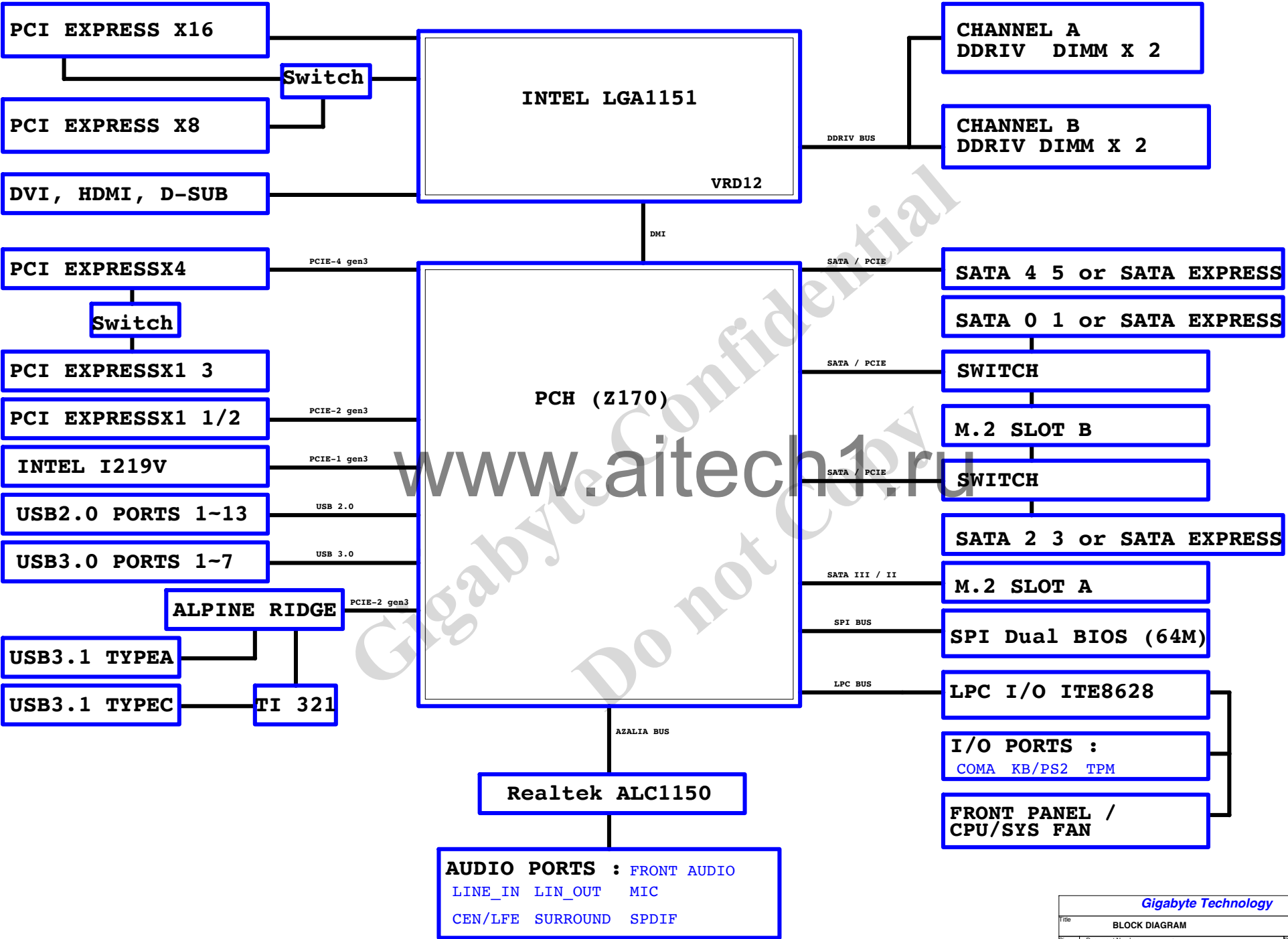
Component value change history

[illegible]

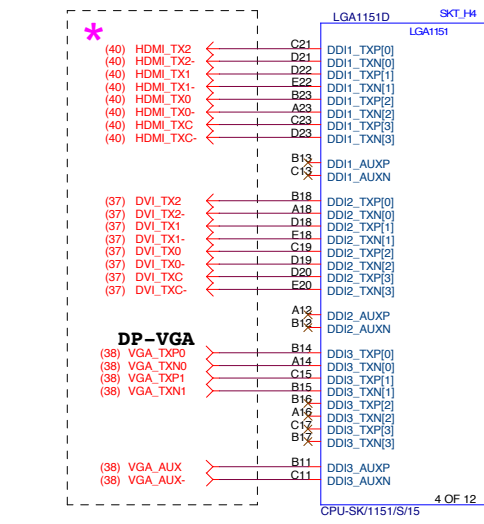
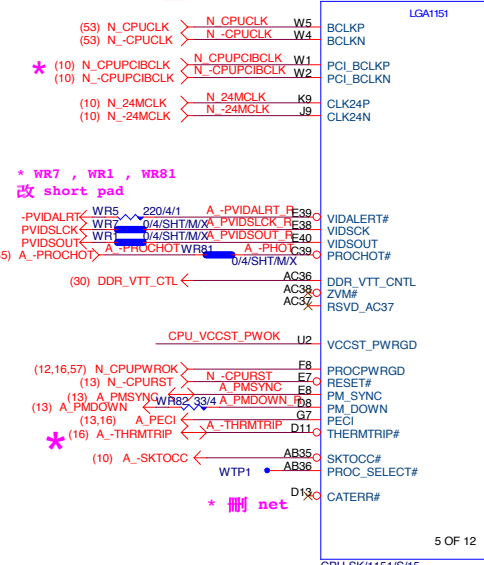
Circuit or PCB layout change

DATE	Change Item	Reason
2015/01/21	1.PCB first release 2.線路由GA-Z1704X-SLI-02-0119B.DSN來修改 3. VCORE, VCCGT from Z1704X-UD5 TH 4. add 2nd M.2 5. add PCIE_X1_3 6. add 80port remove LPT 7. 改架高USB3 8. del turbo key 9. add 後窗裝甲 10. del PCI	REV 0.1
2015/03/24	1. update DP to VGA module (1.03 to 1.05) 2. update discrete power (0.41 to 0.51) 3. update IO module (1.04 to 1.06) 4. remove original HDMI2.0 and TYPE C 5. remove IO shield, GL850 6. add TBT circuit(USB3.1, HDMI 1.4)	REV 0.2
2015/04/02	1. rename Z170X-UD3 0.1	REV 0.1
2015/05/06	1. update TBT module (add TCAR20, THR44 change to 0402, remove THD3) 2. update DVI module(remove VD1) 3. update DP to VGA module(remove DVD1,add DVR21) 4. change PCIE_X16, X8, X4 footprint 5. update DDR VPP module(add MAC49.MAC50.MAC51.MAC52) 6. update PCIE_X4 module(SWAP PPU1 signals, slot 多一pin B48) 7. Q21 change to short pad 8. update FAN module(FNR6 change footprint to FUSE-0603-SHORT10 9. update PCH power module(ADD NPD1.NPD2.NPR22) 10. update DDR module(Modify MR22,MR23,MR25 footprint 11. update LAN module(add LAQ1, LAQR1)	REV 0.2
2015/06/11	1. add DVD1, VD1, THD3, NR3 2. 刪 WR100、WR101、NR302、NR303、WR102、WR103、NR300、NR301 3. U6 change location to DB_PORT 4. RN12, RN13, R199 change location to DB_PRN1, DB_PRN2(改0402 排組), DB_PR1 5. TCA(B)Q3更改為TCA(B)Q1/2 6. PCH.BA4 改接NR7 7. 修改NX1 Layout 8. THC63,THC62,THC65,THC64 9. add HDMI level shifter 10. change Etron to TI	REV 0.3
2015/06/25	1. 刪除VDDSPD 2. NPR22改0805 3. add NPC10 請放置CHOKe一出來的地方 4. WR94改0402 5. add DFC3 close to CPU 6. Add MA_DR9 close to MA_DQ2	REV 9.0

BLOCK DIAGRAM

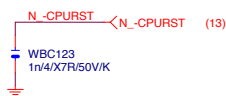


From SKL_0.2B

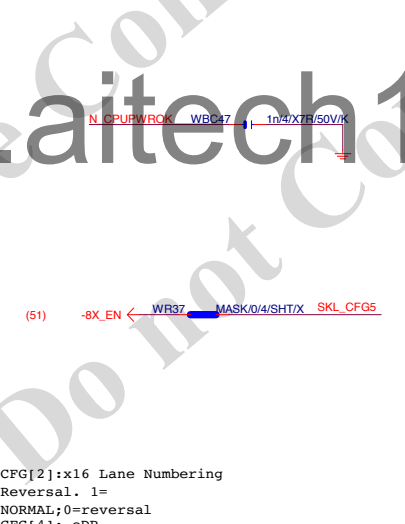
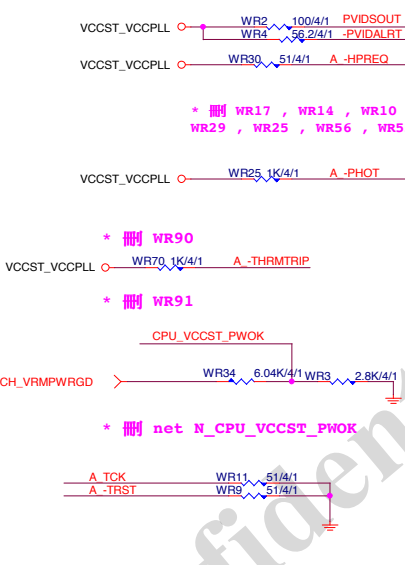
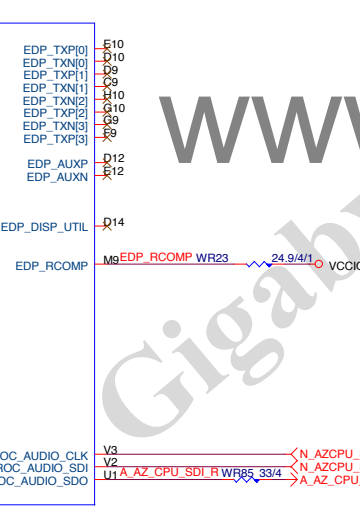
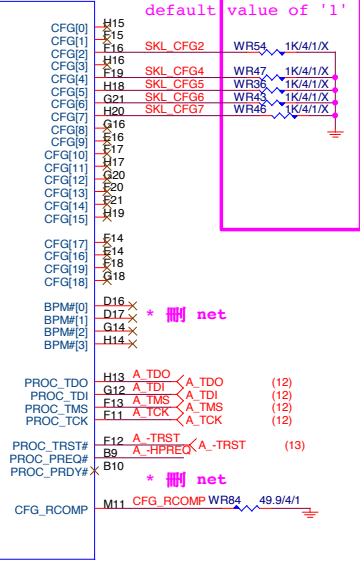


G-15u : (CPU-SK/1151/S/15)
10SC1-F01151-11R / 10SC1-F01151-12R
G-FL : (CPU-SK/1151/S/GF)
10SC1-F01151-21R / 10SC1-F01151-22R

-CPURST

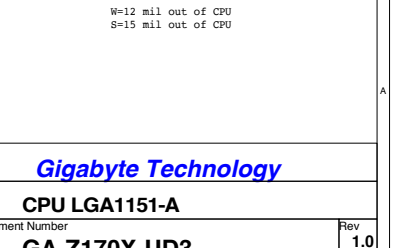
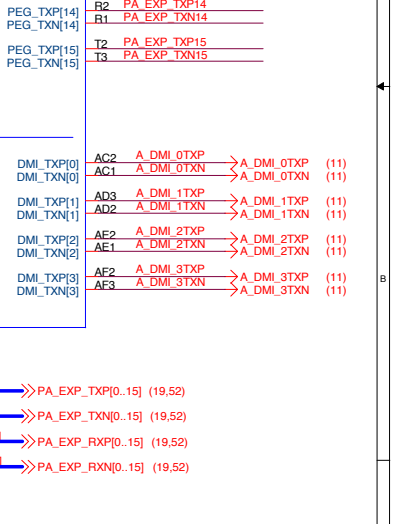
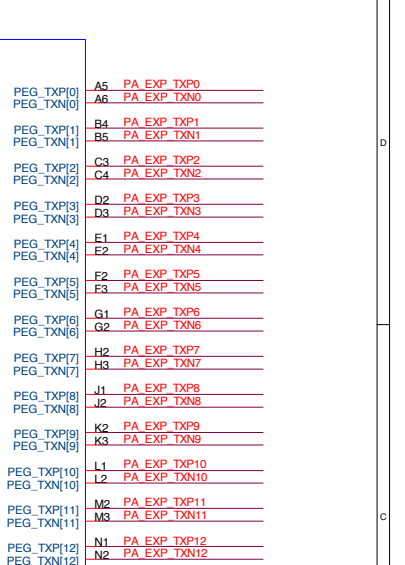
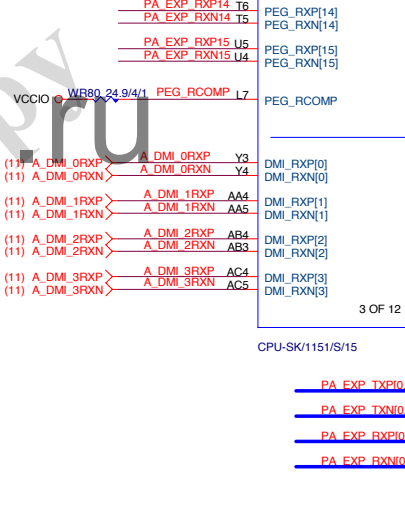
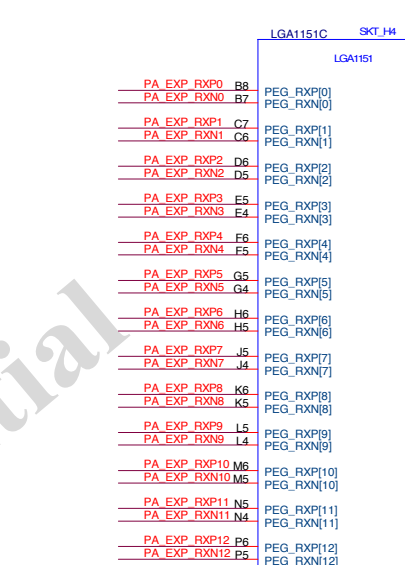


檢查組態調整線路
The CFG signals
default value of '1'

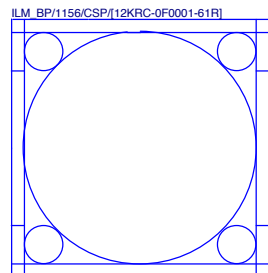


CFG[6,5]:PCI Express* Bifurcation; 1=
1 x16 PCI Express;10=2x8 PCI Express
CFG[7]: PEG Training:1=(default) PEG Train
immediately following RESET#;0=PEG Wait
for BIOS

Bifurcation Config.	Signals	Lanes	
	CFG[6]	CFG[5]	CFG[2]
1x16	1	1	1
1x16 Reversed	1	1	0
2x8	1	0	1
2x8 Reversed	1	0	0
1x8+2x4	0	0	1
1x8+2x4 Reversed	0	0	0



* 改DDR4 net



Need check the new CPU ME



(8) MODT A[0..3] \longleftrightarrow MODT A[0..3]

(9) MODT_B[0..3] \longleftrightarrow MODT_B[0..3]

(8) $MDA[0..63] \longleftrightarrow MDA[0..63]$

(9) $\text{MDB}[0..63] \longleftrightarrow \text{MDB}[0..63]$

(8) M-DQSA[0..7] \longleftrightarrow M-DQSA[0..7]

(8) $\text{MAAA}[0..16] \longleftrightarrow \text{MAAA}[0..16]$

(9) MAAB[0..16] \longleftrightarrow MAAB[0..16]

(9) M_DQSB[0..7] \longleftrightarrow M_DQSB[0..7]

(9) $M_DQSB[0..7] \longleftrightarrow M_DQSB[0..7]$

DDR CHANNEL
B

2 OF 12

DDR0_VREF_DQ AC40
DDR1_VREF_DQ AC39 VREF DQB → VREF DQB (9)

DDR_VREF_CA AB40 VREF_CAB → VREF_CAB (8)

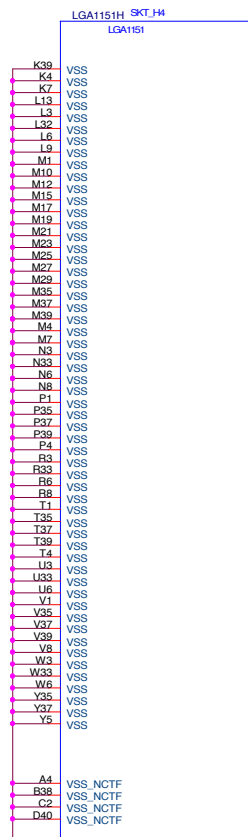
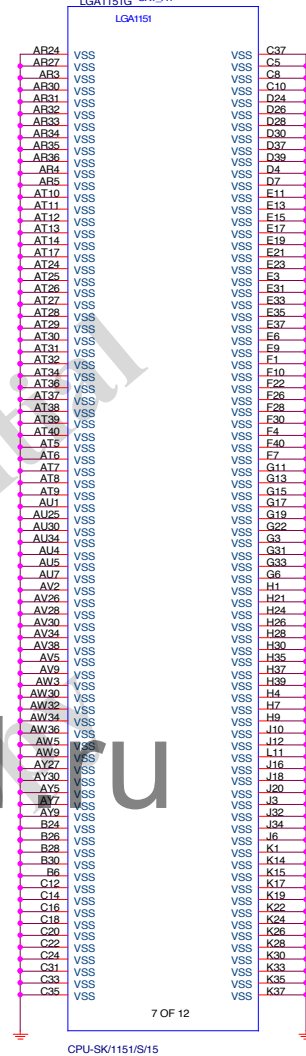
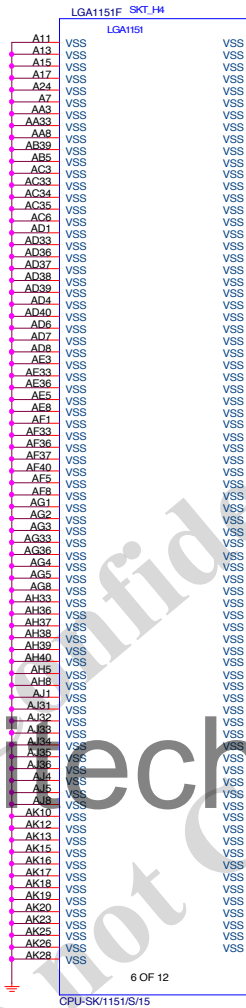
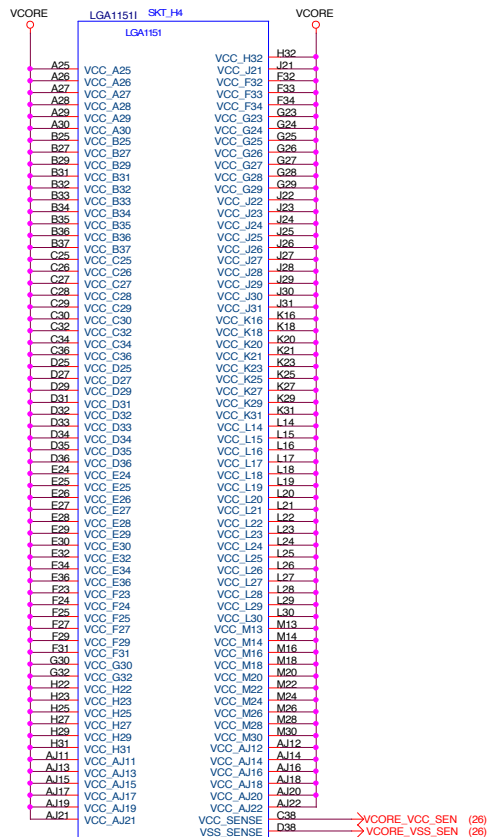
DDR0_VREF_DQ
DDR1_VREF_DQ

AC39 VREF_DQB → VREF_DQB (9)

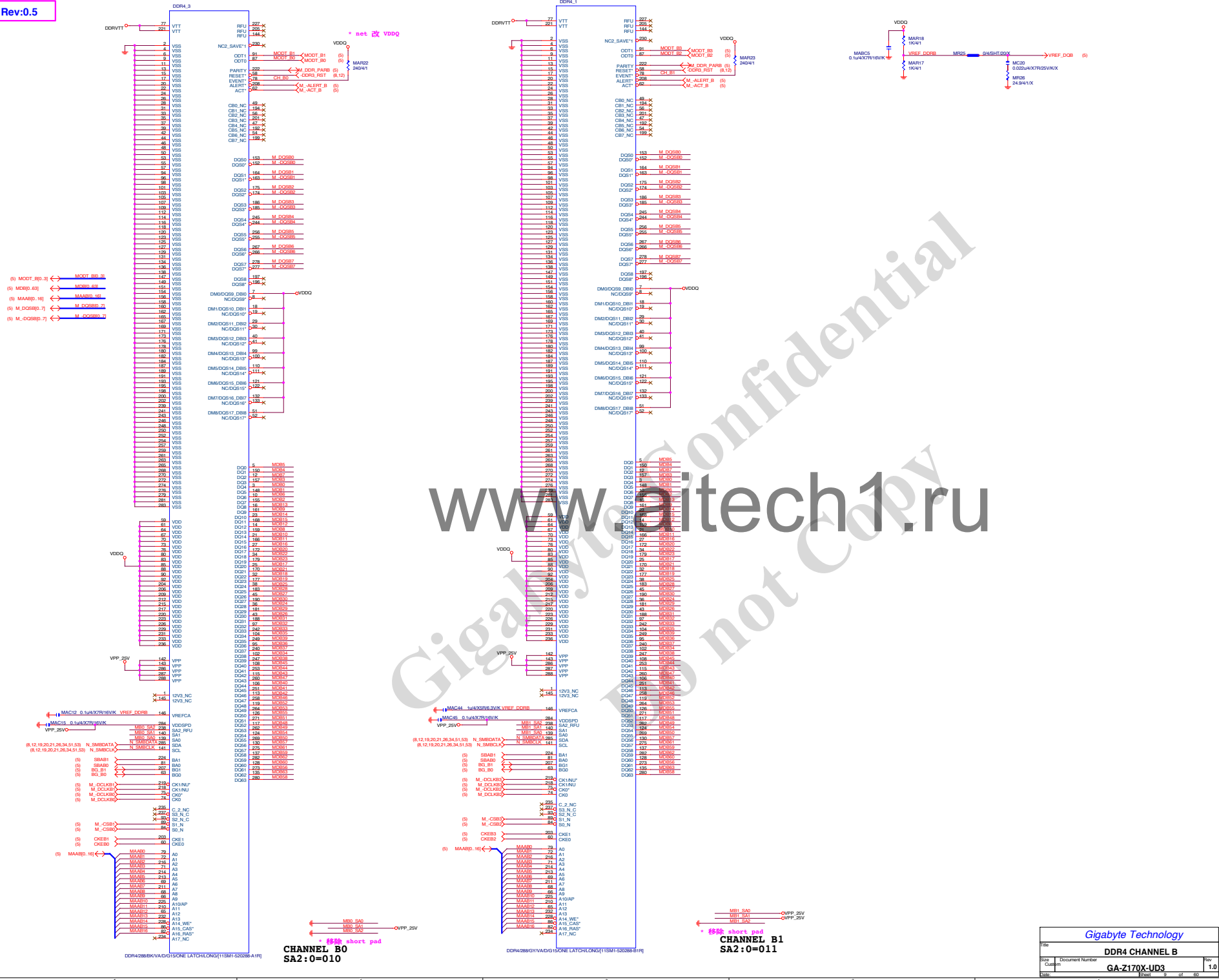
Gigabyte Technology

Title	CPU LGA1151-B
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Size Custom	Document Number GA-7170X-UD3	Rev 1.0
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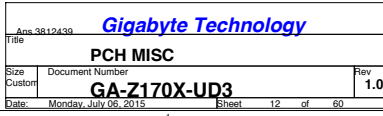


* 刪 Vcore 電容

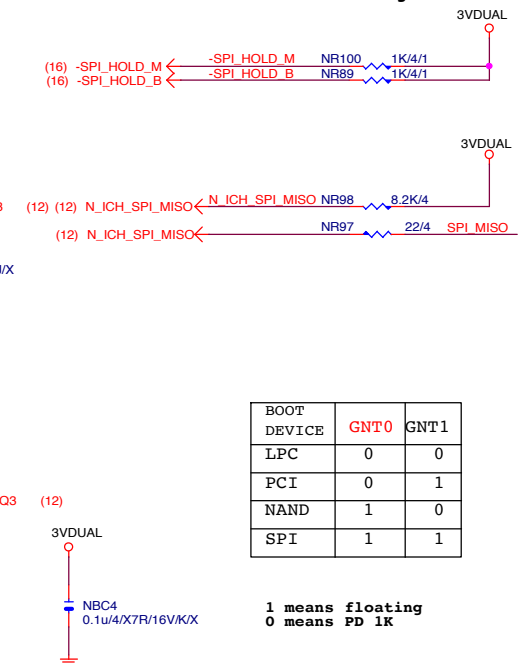
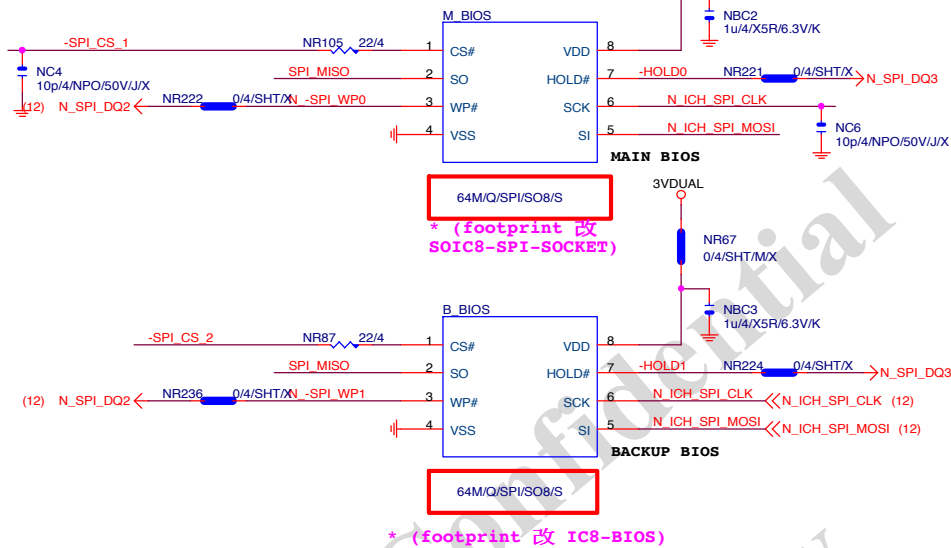


CHANNEL B0
SA2:0=010

CHANNEL B1
SA2:0=011



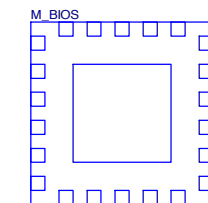
MOSI For DMI RX Termination Voltage



BOOT DEVICE	GNT0	GNT1
LPC	0	0
PCI	0	1
NAND	1	0
SPI	1	1

1 means floating
0 means PD 1K

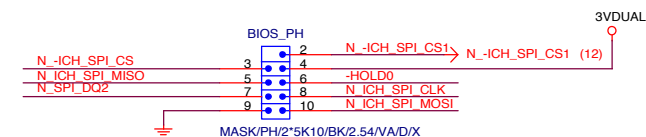
www.aitech1.ru

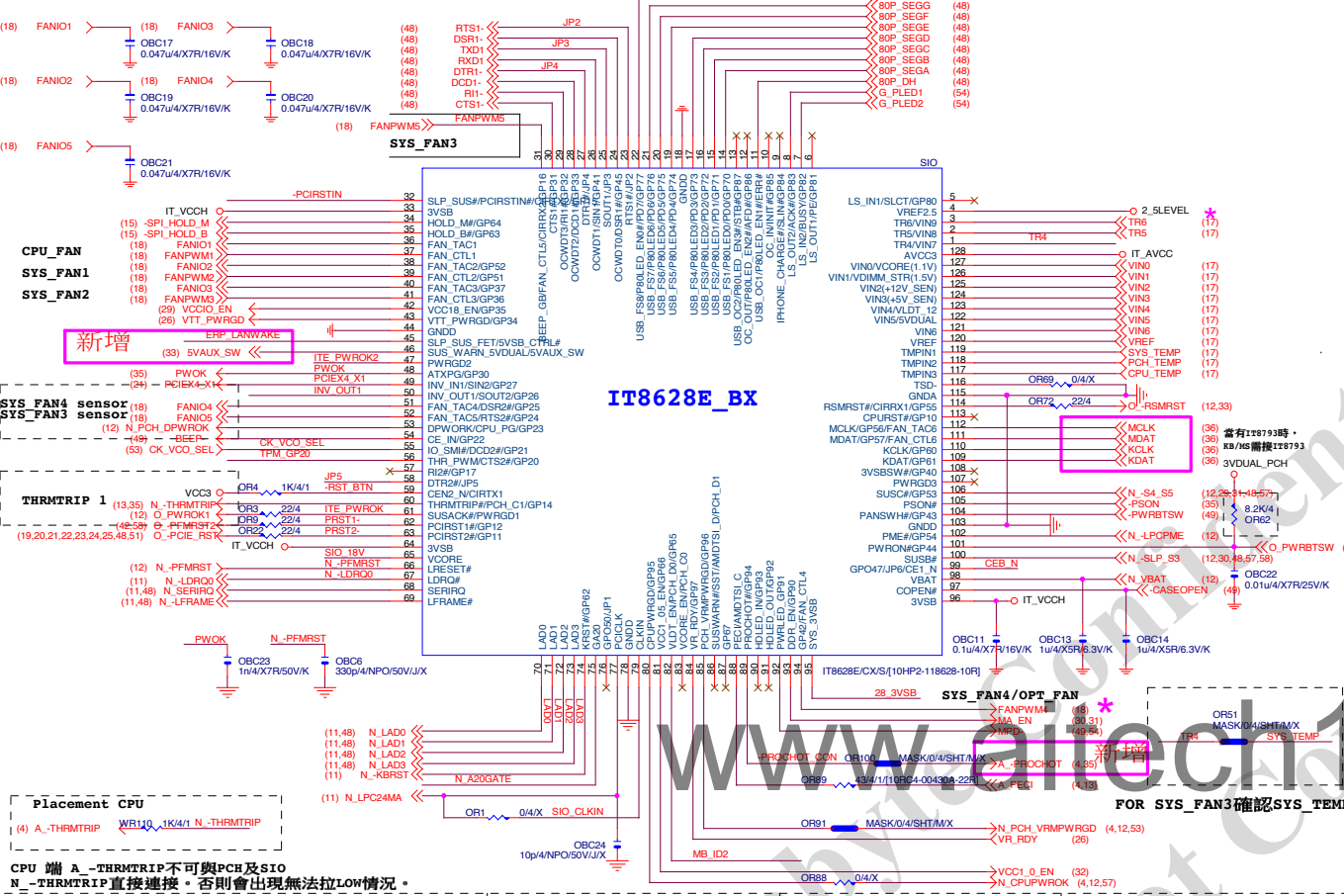


LCP/G-FL/1.27mm/200MIL/WHITE[10SL2-000008-31R]X

* 試產先上，PVT 移除

BIOS_PH

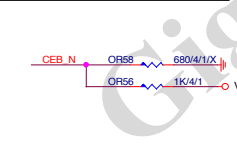




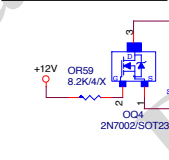
FAN TABLE	
CPU_FAN	FAN_CTL1 FAN_TAC1
SYS_FAN1	FAN_CTL4 FAN_TAC4
SYS_FAN2	FAN_CTL3 FAN_TAC3
SYS_FAN3	FAN_CTL5 FAN_TAC5
OPT FAN or SYS_FAN4	FAN_CTL2 FAN_TAC2
THRMTRIP1	YES PIN60

IT8628E GPIO問題匯整	
PIN 50	GP26-第一次接上POWER時會拉 Lo
PIN 90/91	DEFAULT為HDLed FUNCTION, GP93 BYPASS TO GP92 高運時 GP92 會被拉 Lo (ITE BUG)
PIN 108	GP40--- POWER ON 時會拉 Lo
PIN 111/112	MOUSE 跟FAN6 FUNCTION 擇一使用, 不然會互相干擾
PIN 22	PIN22-, 需高於3V-, 若低於此部分COM PORT及LPT裝置 蜂鳴器會異常動作。

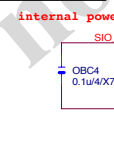
DUAL BIOS OPT STRAP



Power leakage



SIO 18V



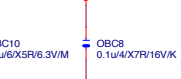
SIO CAP



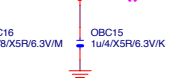
IT_VCCH



IT_AVCC



3VDUAL_PCH

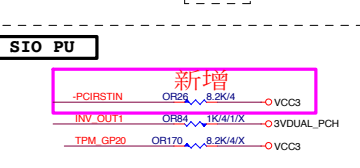


MB ID

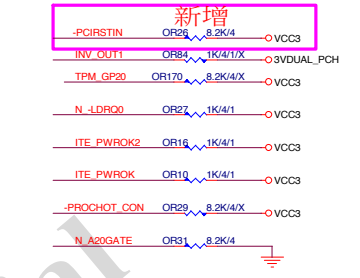


JP2	1	Disable WDT
JP2	0	Enable WDT to rest PWR0K
JP3	1	SPI-Flash Disable
JP3	0	SPI-Flash Enable
JP4	1	k8 power sequency function is Disable
JP4	0	k8 power sequency function is Enable
JP5	1	anti-surge Disable
JP5	0	anti-surge Enable
JP5	1 1	The default value of EC Index 63h/6Bh/73h is 80h.
JP3	1 0	The default value of EC Index 63h/6Bh/73h is FFh
JP5	0 1	The default value of EC Index 63h/6Bh/73h is 00h.
JP5	0 0	The default value of EC Index 63h/6Bh/73h is 40h.

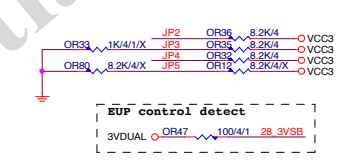
PWR SHT



SIO PU



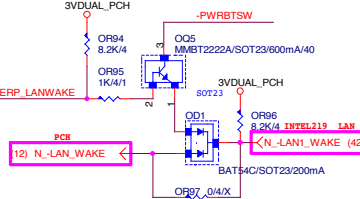
SIO STRAP



ERP WAKE on LAN (依LAN組態選擇)

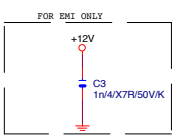
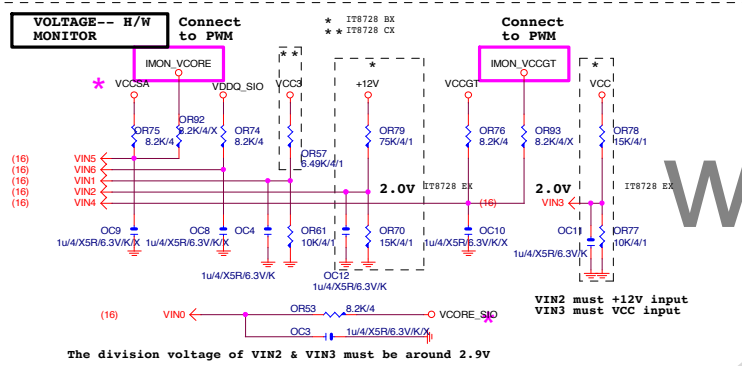
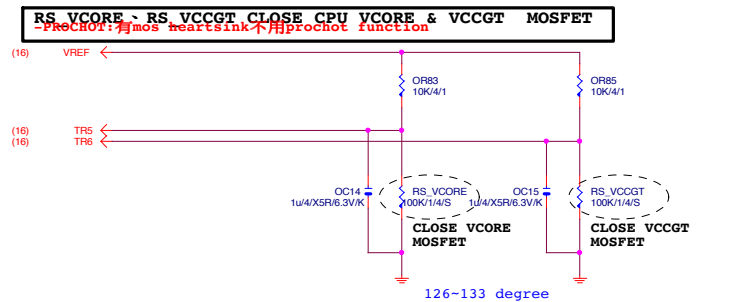
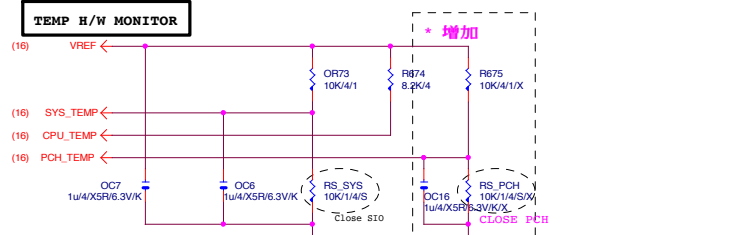


(組態二) Intel LAN

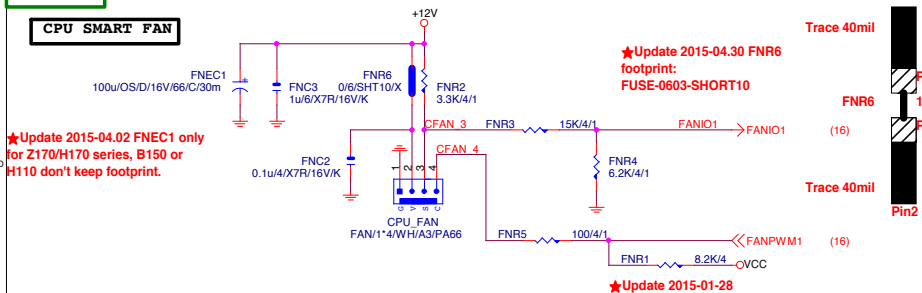


ERP Wake on LAN		
Single LAN	Realtek	組態一
	Atheros	組態二
Dual LAN	Intel 219	組態一
	Atheros+Atheros	組態二
No Support ERP	Intel 219+Intel 210	組態三
	BOM不上	N/A

Gigabyte Technology		
ITE 8620 LPC IO		
GA-Z170X-UD3		
Date:	Monday, July 06, 2015	Sheet 16 of 60



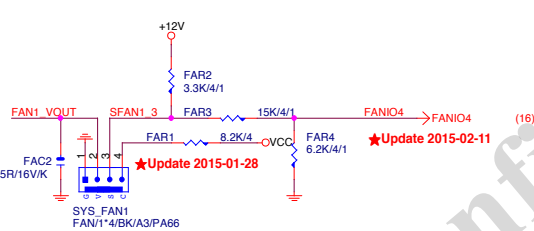
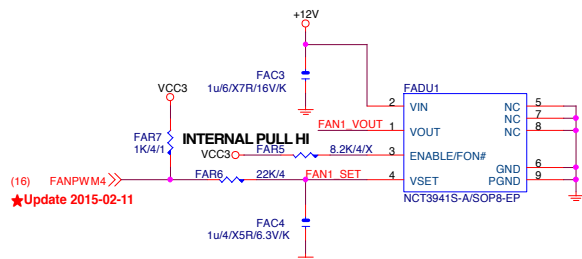
CPU SMART FAN



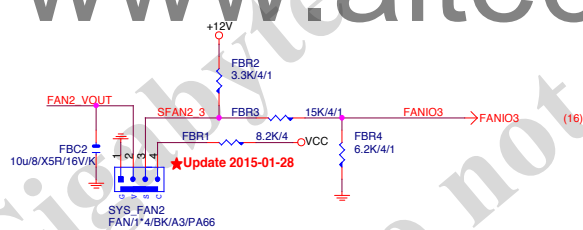
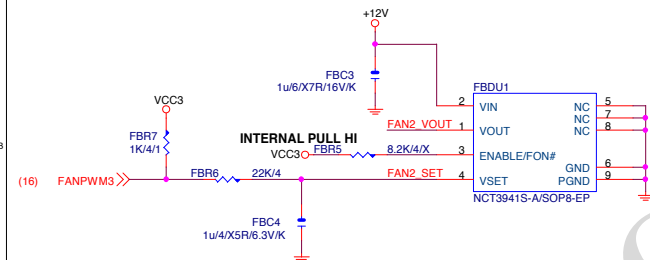
SYSTEM FAN1

Linear SYS FAN

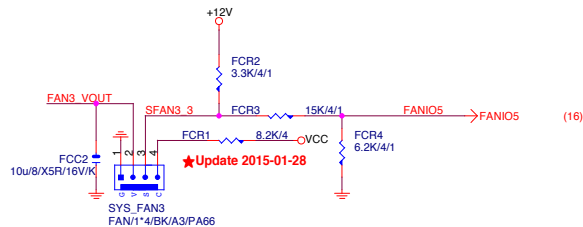
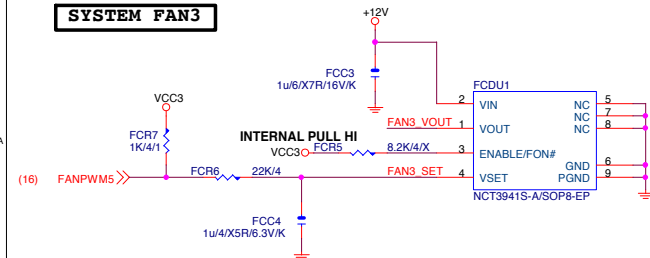
Enable Function (NCT3941S)
Full Turn On Function (NCT3941S-A)



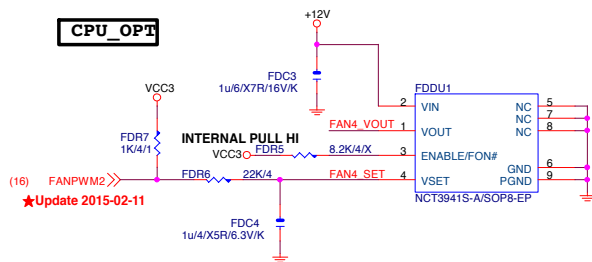
SYSTEM FAN2



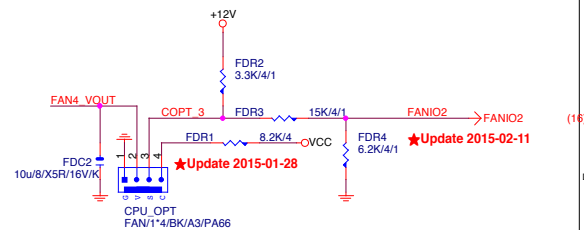
SYSTEM FAN3



CPU_OPT



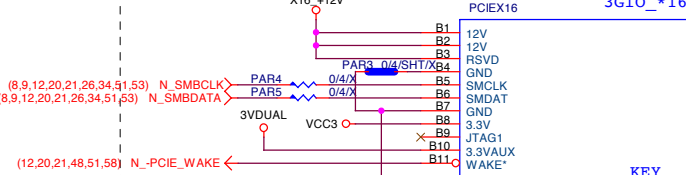
SYSTEM FANX



PCIEX16 CAP

PCIEX16 SLOT

PCIESLOT-164DN-Q

**PCIEX16 PROTECT SHT**

PCIEX16 AC CAP

PA EXP TXP0	PA05	0.22uA/4X5R6.3V/K	PA EXP TXP0 C
PA EXP TXN0	PA04	0.22uA/4X5R6.3V/K	PA EXP TXN0 C
PA EXP TXP1	PA06	0.22uA/4X5R6.3V/K	PA EXP TXP1 C
PA EXP TXN1	PA07	0.22uA/4X5R6.3V/K	PA EXP TXN1 C
PA EXP TXP2	PA08	0.22uA/4X5R6.3V/K	PA EXP TXP2 C
PA EXP TXN2	PA09	0.22uA/4X5R6.3V/K	PA EXP TXN2 C
PA EXP TXP3	PA010	0.22uA/4X5R6.3V/K	PA EXP TXP3 C
PA EXP TXN3	PA011	0.22uA/4X5R6.3V/K	PA EXP TXN3 C
PA EXP TXP4	PA012	0.22uA/4X5R6.3V/K	PA EXP TXP4 C
PA EXP TXN4	PA013	0.22uA/4X5R6.3V/K	PA EXP TXN4 C
PA EXP TXP5	PA014	0.22uA/4X5R6.3V/K	PA EXP TXP5 C
PA EXP TXN5	PA015	0.22uA/4X5R6.3V/K	PA EXP TXN5 C
PA EXP TXP6	PA016	0.22uA/4X5R6.3V/K	PA EXP TXP6 C
PA EXP TXN6	PA017	0.22uA/4X5R6.3V/K	PA EXP TXN6 C
PA EXP TXP7	PA018	0.22uA/4X5R6.3V/K	PA EXP TXP7 C
PA EXP TXN7	PA019	0.22uA/4X5R6.3V/K	PA EXP TXN7 C
PA EXP SW TXP8 C	PA021	0.22uA/4X5R6.3V/K	PA EXP SW TXP8 C
PA EXP SW TXN8 C	PA020	0.22uA/4X5R6.3V/K	PA EXP SW TXN8 C
PA EXP SW TXP9 C	PA022	0.22uA/4X5R6.3V/K	PA EXP SW TXP9 C
PA EXP SW TXN9 C	PA021	0.22uA/4X5R6.3V/K	PA EXP SW TXN9 C
PA EXP SW TXP10 C	PA024	0.22uA/4X5R6.3V/K	PA EXP SW TXP10 C
PA EXP SW TXN10 C	PA025	0.22uA/4X5R6.3V/K	PA EXP SW TXN10 C
PA EXP SW TXP11 C	PA026	0.22uA/4X5R6.3V/K	PA EXP SW TXP11 C
PA EXP SW TXN11 C	PA027	0.22uA/4X5R6.3V/K	PA EXP SW TXN11 C
PA EXP SW TXP12 C	PA028	0.22uA/4X5R6.3V/K	PA EXP SW TXP12 C
PA EXP SW TXN12 C	PA029	0.22uA/4X5R6.3V/K	PA EXP SW TXN12 C
PA EXP SW TXP13 C	PA030	0.22uA/4X5R6.3V/K	PA EXP SW TXP13 C
PA EXP SW TXN13 C	PA031	0.22uA/4X5R6.3V/K	PA EXP SW TXN13 C
PA EXP SW TXP14 C	PA032	0.22uA/4X5R6.3V/K	PA EXP SW TXP14 C
PA EXP SW TXN14 C	PA033	0.22uA/4X5R6.3V/K	PA EXP SW TXN14 C
PA EXP SW TXP15 C	PA034	0.22uA/4X5R6.3V/K	PA EXP SW TXP15 C
PA EXP SW TXN15 C	PA035	0.22uA/4X5R6.3V/K	PA EXP SW TXN15 C

The diagram illustrates the pin-to-pin mapping between the PCIEX16 and X16_12Z connectors. It shows 120 pins on each side, with various signals like RSVD, GND, HSON, HSI, and PA EXP. The diagram includes a 'KEY' section in the middle and a large watermark 'www.aitech.ru' across the center.

PCIEX16	Signal	X16_12Z
B1	12V	A1
B2	12V	A2
B3	RSVD	A3
B4	GND	A4
B5	SMCLK	A5
B6	SMDAT	A6
B7	GND	A7
B8	3.3V	A8
B9	JTAG1	A9
B10	3.3VAUX	A10
B11	WAKE*	A11
B12	RSVD	A12
B13	GND	A13
B14	HSON0	A14
B15	HSON0	A15
B16	GND	A16
B17	PRSN2*	A17
B18	GND	A18
B19	HSOP1	A19
B20	HSON1	A20
B21	GND	A21
B22	GND	A22
B23	HSOP2	A23
B24	HSON2	A24
B25	GND	A25
B26	GND	A26
B27	HSOP3	A27
B28	HSON3	A28
B29	GND	A29
B30	RSVD	A30
B31	PRSN2*	A31
B32	GND	A32
B33	HSOP4	A33
B34	HSON4	A34
B35	GND	A35
B36	GND	A36
B37	HSOP5	A37
B38	HSON5	A38
B39	GND	A39
B40	GND	A40
B41	HSOP6	A41
B42	HSON6	A42
B43	GND	A43
B44	GND	A44
B45	HSOP7	A45
B46	HSON7	A46
B47	GND	A47
B48	PRSN2*	A48
B49	GND	A49
B50	HSOP8	A50
B51	HSON8	A51
B52	GND	A52
B53	GND	A53
B54	HSOP9	A54
B55	HSON9	A55
B56	GND	A56
B57	GND	A57
B58	HSOP10	A58
B59	HSON10	A59
B60	GND	A60
B61	GND	A61
B62	HSOP11	A62
B63	HSON11	A63
B64	GND	A64
B65	GND	A65
B66	HSOP12	A66
B67	HSON12	A67
B68	GND	A68
B69	GND	A69
B70	HSOP13	A70
B71	HSON13	A71
B72	GND	A72
B73	GND	A73
B74	HSOP14	A74
B75	HSON14	A75
B76	GND	A76
B77	GND	A77
B78	HSOP15	A78
B79	HSON15	A79
B80	GND	A80
B81	PRSN2*	A81
B82	RSVD	A82

PCIEX16:16/5/5/5/16

PA_EXP_RXP[0..15] \gg PA_EXP_RXP[0..15] (4,52)

PA_EXP_RXN[0..15] >> PA_EXP_RXN[0..15] (4,52)

PA_EXP_TXP[0..15] >> PA_EXP_TXP[0..15] (4,52)

PA_EXP_TXN[0..15] \gg PA_EXP_TXN[0..15] (4,52)

PA_EXP_SW_RXP[8..15] \gg PA_EXP_SW_RXP[8..15] (52)

PA_EXP_SW_RXN[8..15] >> PA_EXP_SW_RXN[8..15] (52)

PA EXP SW TXP[8..15] >> PA EXP SW TXP[8..15] (52)

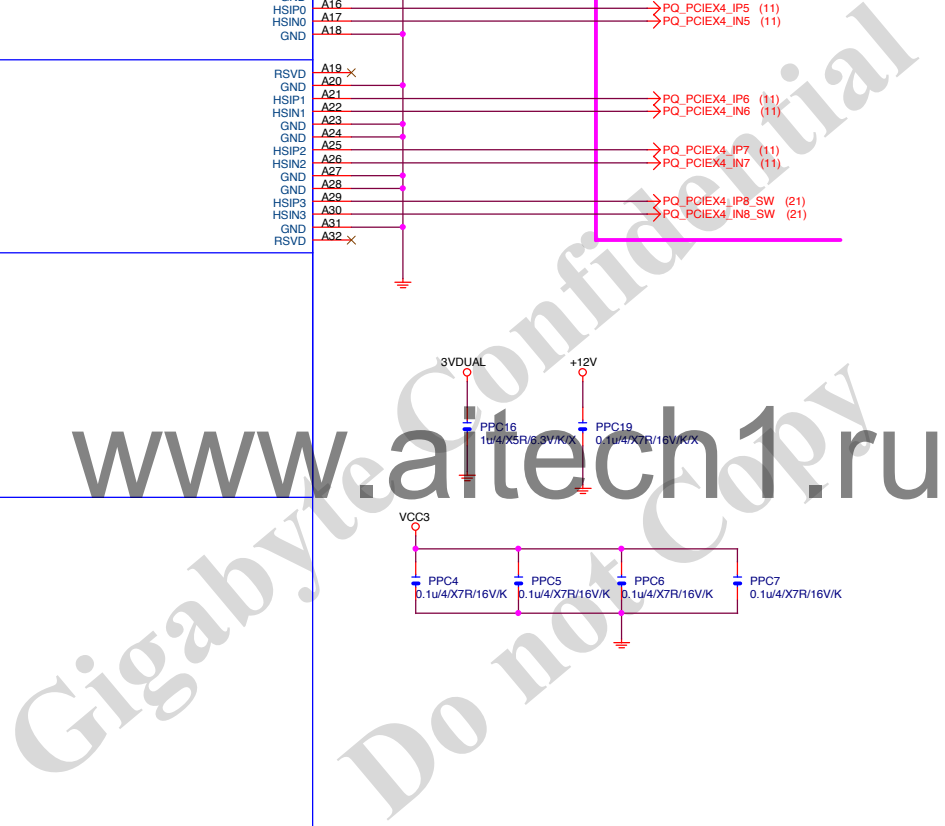
PA EXP SW TXN[8..15] >> PA EXP SW TXN[8..15] (52)

PCI-E REV:2.0--> 5GHZ

Gigabyte Technology

PCI EXPRESS * 16

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M.2 Lane4 from PCH port18

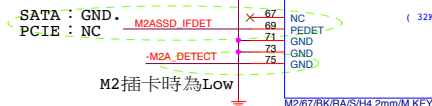
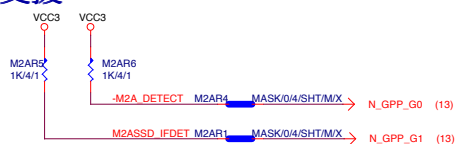
M.2 Lane3 from PCH port17

M.2 Lane2 from PCH port16

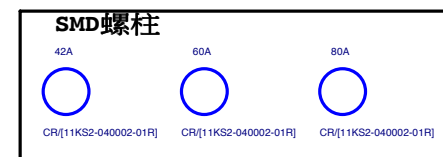
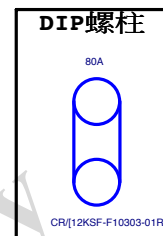
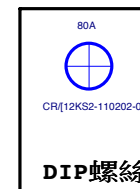
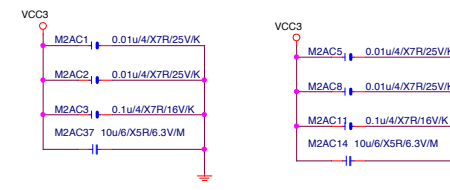
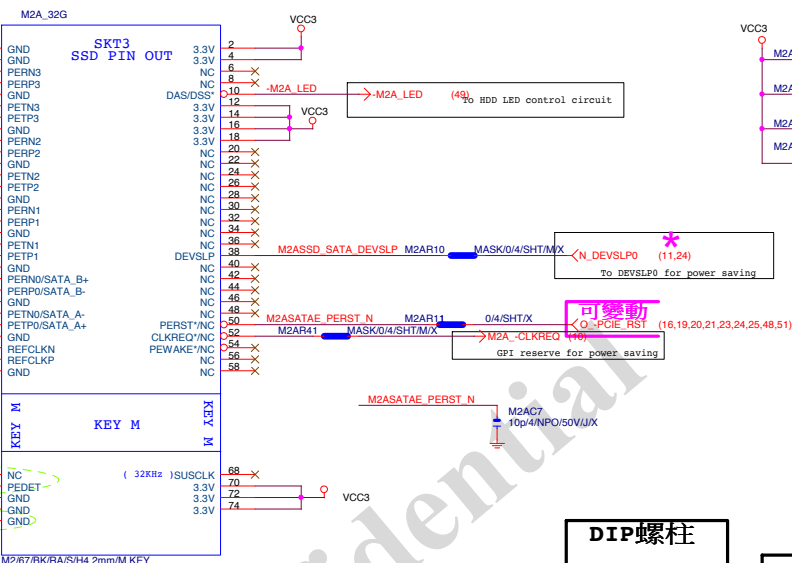
M.2 Lane2 from PCH port15

需與M2_-CLKREQ對應

支援SATA and M.2 function



M2插卡時為Low



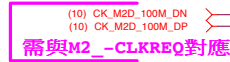
M.2 有插卡 /沒插卡 GPP_G0	M.2插何種卡? GPP_G1	SATA Express 插何種硬碟? GPP_E0/E2/F1	IO15 (S0)	IO16 (S1)	IO17	IO18	IO19 (S0)	IP20 (S1)
有插卡 (Low)	SATA Mode (Low)	SATA (Hi)	SATA (M.2)	PCIE x1	PCIE x1	PCIE x1	PCIE x1	SATA
		SATA Express (Low)	SATA (M.2)	PCIE x1	PCIE x1	PCIE x1	SATA Express	
	PCIE Mode (Hi)	SATA (Hi)	PCIE x4 (For M.2)				SATA	SATA
		SATA Express (Low)	PCIE x4 (For M.2)				SATA Express	
沒插卡 (Hi)	Don't Care (Hi)	SATA (Hi)	PCIE x4				SATA	SATA
		SATA Express (Low)	PCIE x4				SATA Express	

M.2 Lane2 from PCH port19

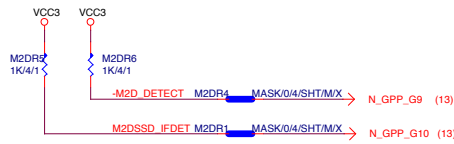
M.2 Lane2 from PCH port20

M.2 Lane3 from PCH port21

M.2 Lane4 from PCH port22



支援SATA and M.2 function



M.2-SATA (S3)+SATA S0&S1&S2

WHEN	PCH GPIO	SETUP	SWITCH
GPP_G9	L	GPP_C20	L
GPP_G10	L	GPP_C19	L
GPP_E0/E1/E2/F0	H (SATA)	GPP_C21	H

M.2-SATA(S3)+S.E.D(S0+S1)

WHEN	PCH GPIO	SETUP	SWITCH
GPP_G9	L	GPP_C20	L
GPP_G10	L	GPP_C19	L
GPP_E0/E1/E2/F0	L (S.E.)	GPP_C21	H

M. 2x4

WHEN	PCH GPIO	SETUP	SWITCH
GPP_G9	L	GPP_C20	H
GPP_G10	H	GPP_C19	H
GPP_E0/E1/E2/F0	H	GPP_C21	H

M.2X2+S.E.D(S0+S1)

WHEN	PCH GPIO	SETUP	SWITCH
GPP_G9	L	GPP_C20	H
GPP_G10	H	GPP_C19	H
GPP_E0/E1/E2/F0	L	GPP_C21	H

M.2X2+SATA S0&S1

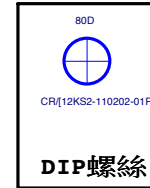
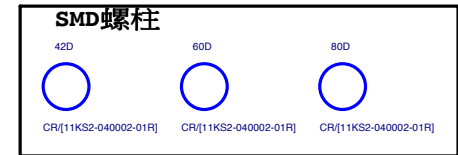
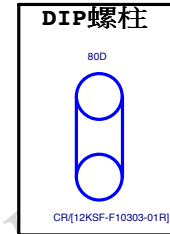
WHEN	PCH GPIO	SETUP	SWITCH
GPP_G9	L	GPP_C20	H
GPP_G10	H	GPP_C19	H
GPP_E0/E1/E2/F0	H	GPP_C21	H

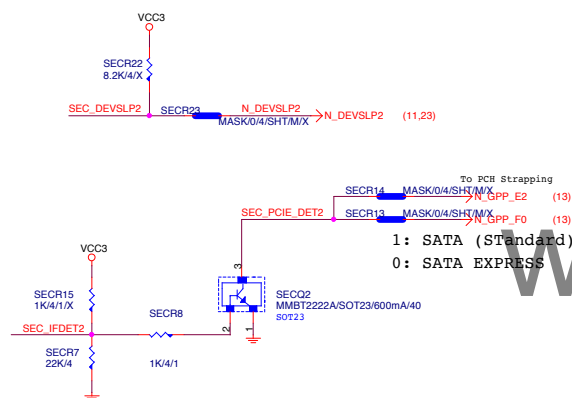
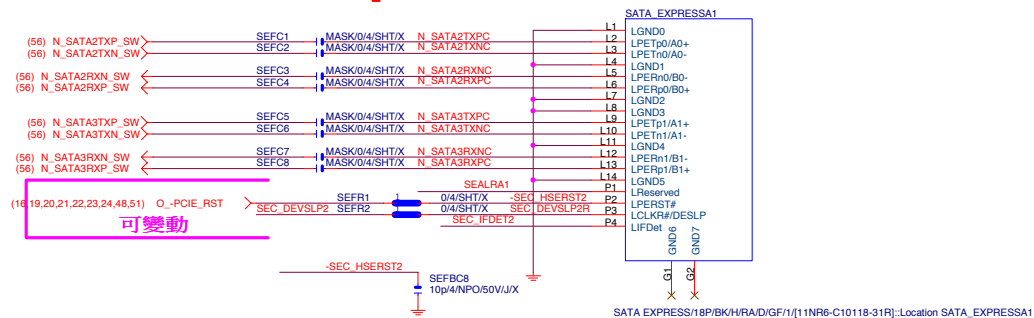
M.2沒插卡+SATA S0-S3

WHEN	PCH GPIO	SETUP	SWITCH
GPP_G9	H	GPP_C20	L
GPP_G10	H	GPP_C19	L
GPP_E0/E1/E2/F0	H	GPP_C21	L

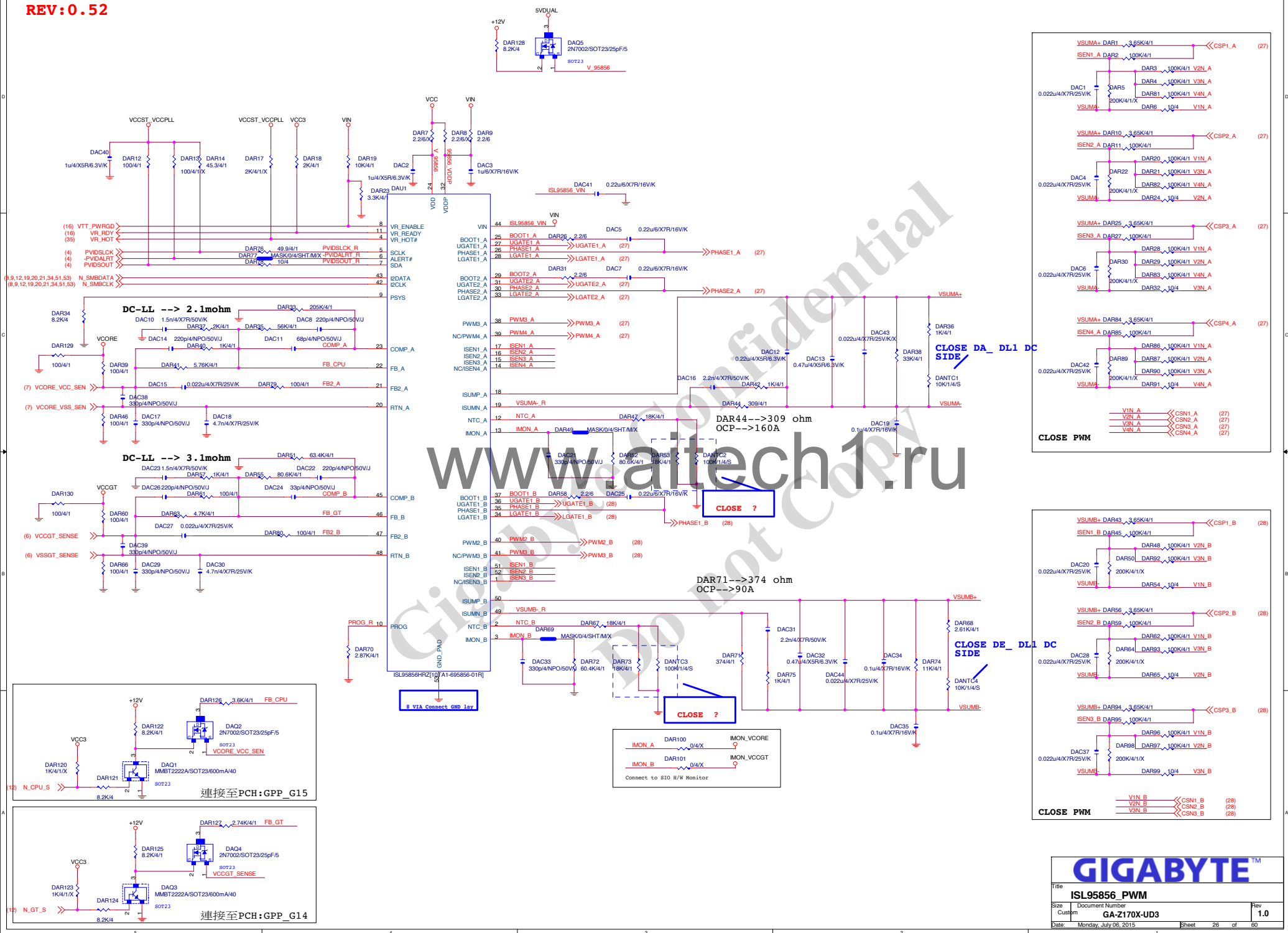
M.2沒插卡+S.E.C&S.E.D

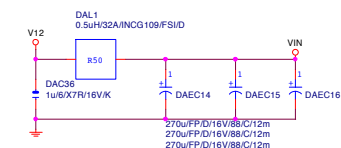
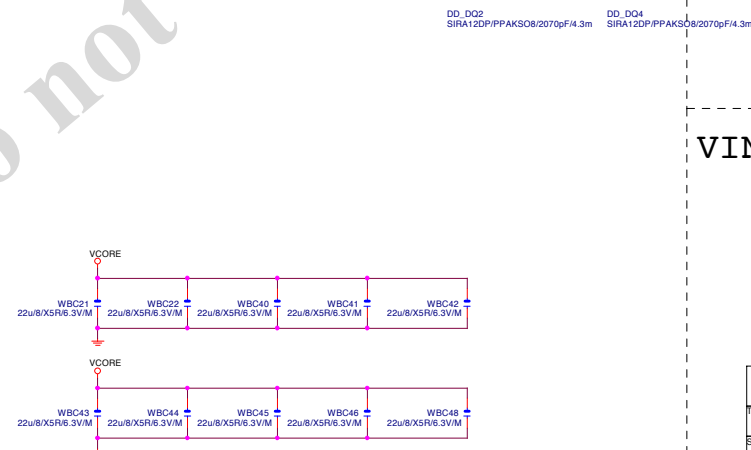
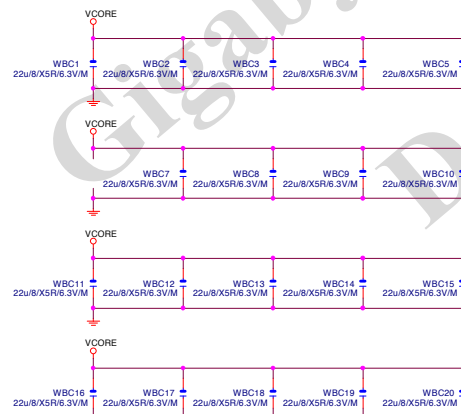
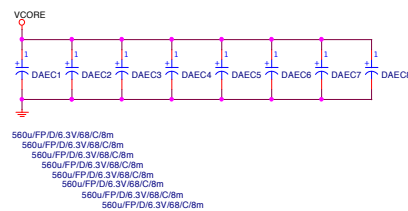
WHEN	PCH GPIO	SETUP	SWITCH
GPP_G9	H	GPP_C20	L
GPP_G10	H	GPP_C19	L
GPP_E0/E1/E2/F0	L	GPP_C21	L



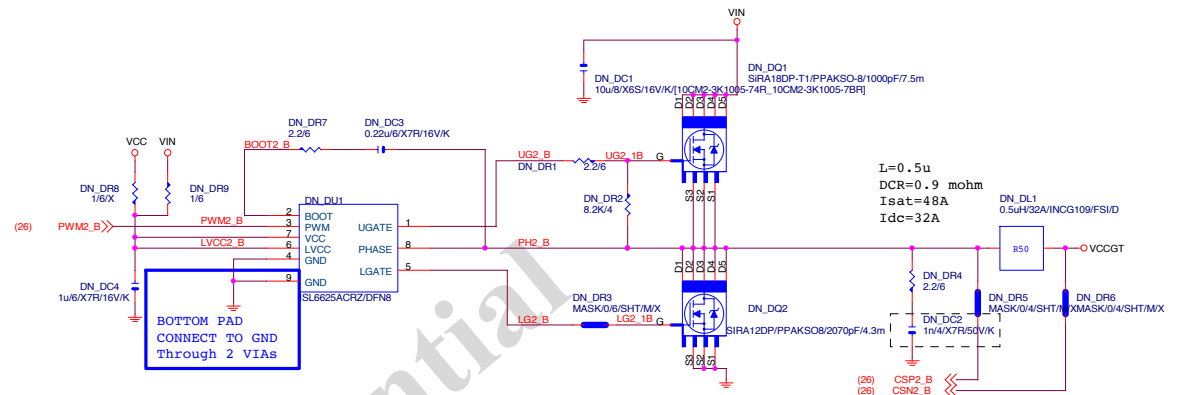
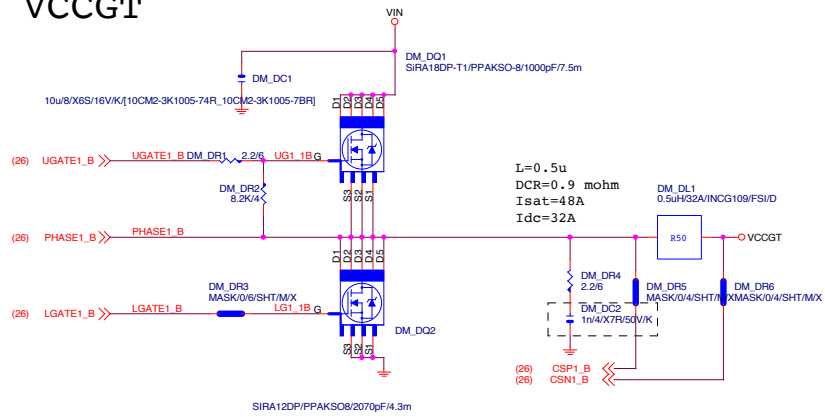
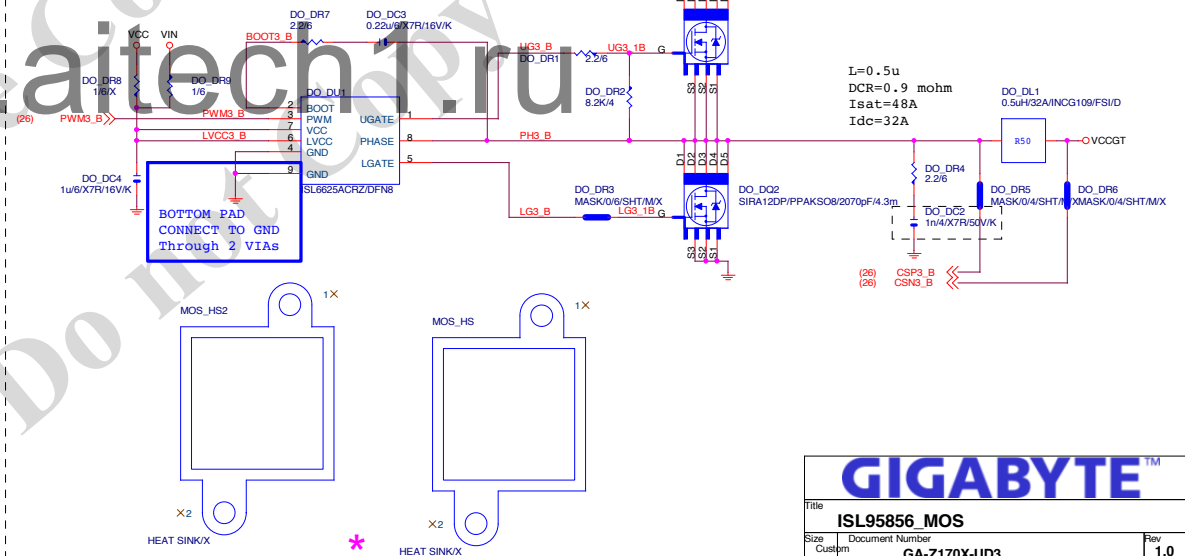
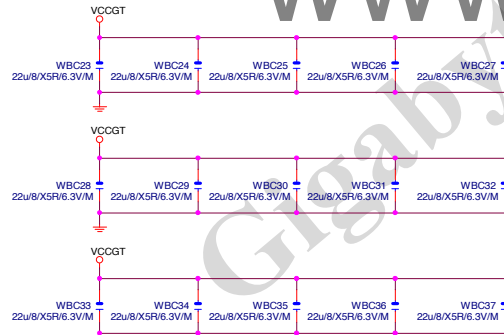
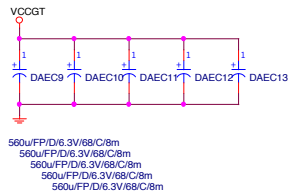
SATA EXPRESS 下層 To SATA3
port2/3

SATA 5 (文字面寫SATA 1)
SATA 4 (文字面寫SATA 0)
SATA 3
SATA 2
SATA 1 (文字面寫SATA 5)
SATA 0 (文字面寫SATA 4)





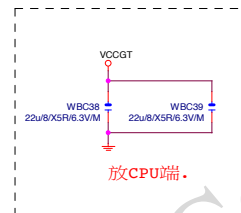
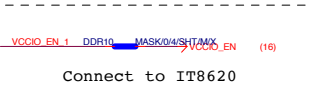
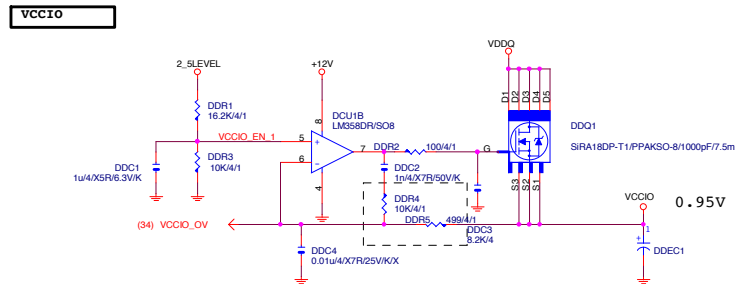
VCCGT

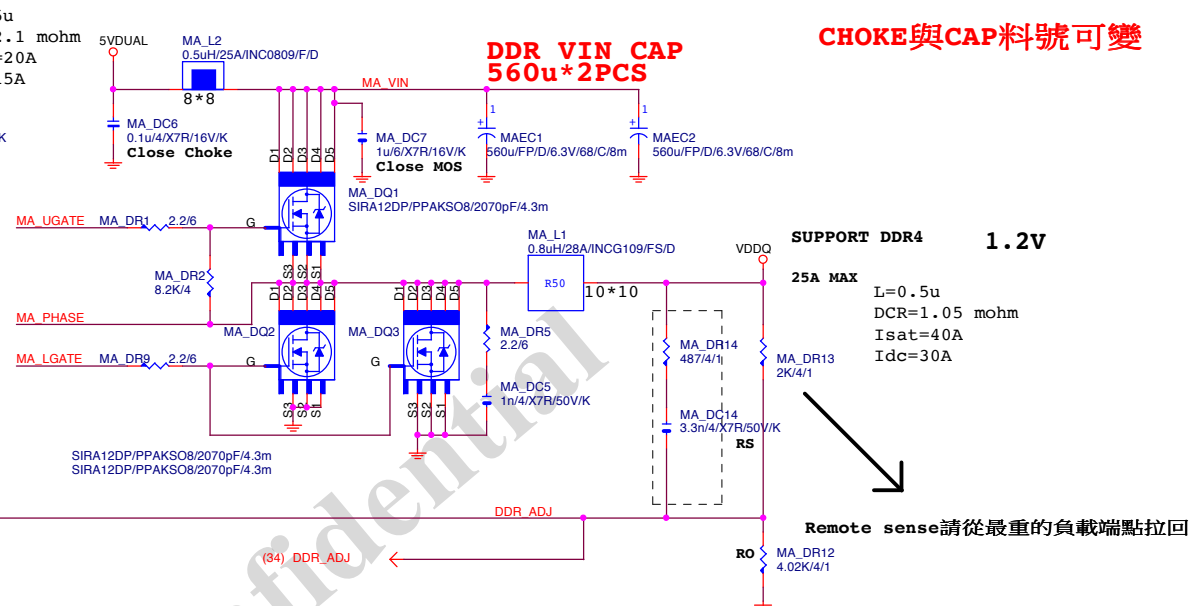
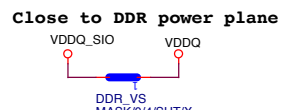
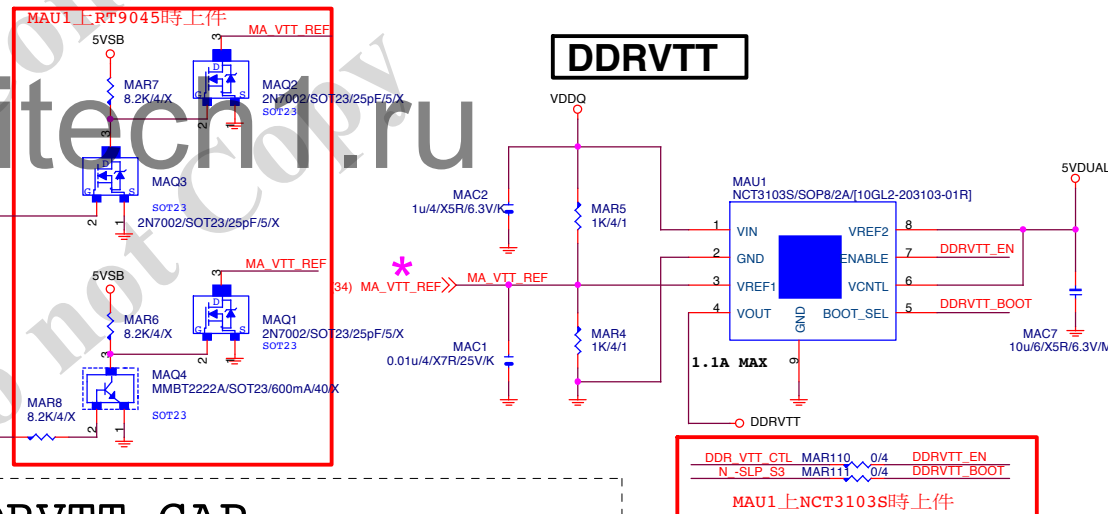
VCCGT CAP 560u*5PCS
22u*15PCS

GIGABYTE™

Title		
ISL95856 MOS		
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VCCSA



[illegible]

VDDQ

1

MAEC3
560uF/P/D/6.3V/68/C/8m

VDDQ

1

MAEC4
560uF/P/D/6.3V/68/C/8m

* 大電容 x4

VDDQ

1

MAEC6
560uF/P/D/6.3V/68/C/8m

VDDQ

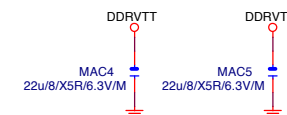
1

MAEC7
560uF/P/D/6.3V/68/C/8m

WBC49
22u/8/X5R/6.3V/M

WBC6
22u/8/X5R/6.3V/M

* 大電容 x0

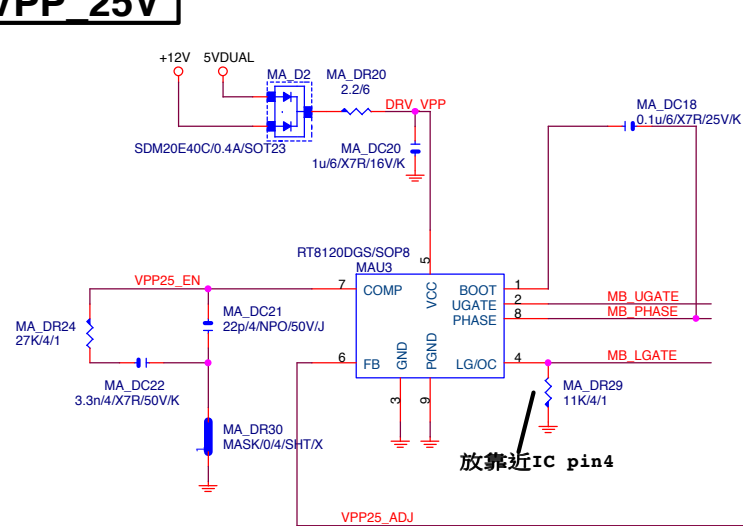


GIGABYTE™

Title			
RT8120_ DDR4 POWER			
Size	Document Number	Rev	
Custom	GA-Z170X-UD3	1.0	
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REV:0.84

VPP_25V

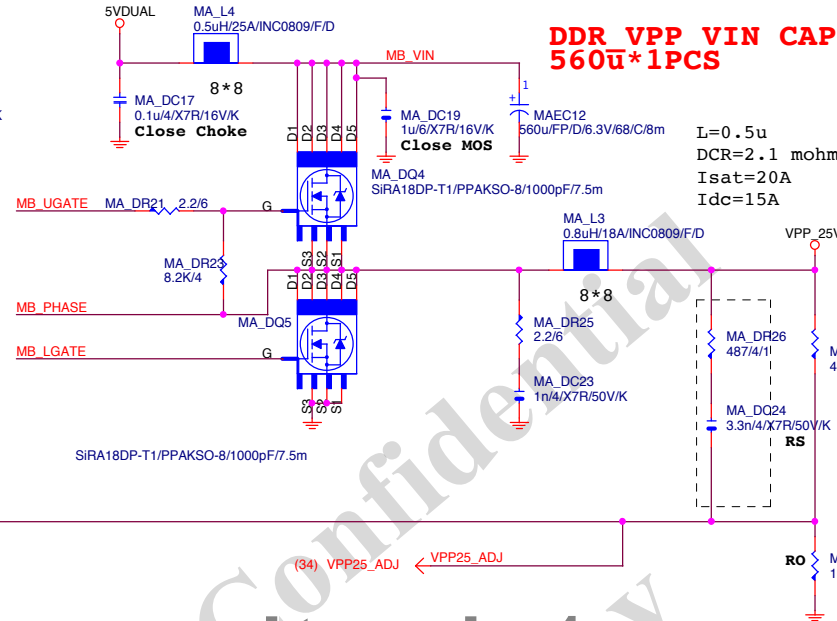


放靠近IC pin4

L=0.5u
DCR=2.1 mohm
Isat=20A
Idc=15A

CHOKE與CAP料號可變

DDR VPP VIN CAP
560u*1PCS



L=0.5u
DCR=2.1 mohm
Isat=20A
Idc=15A

SUPPORT DDR4 2.5V

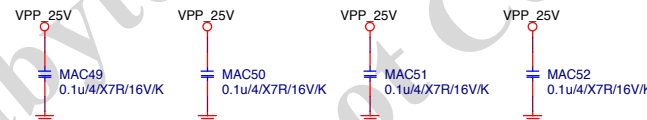
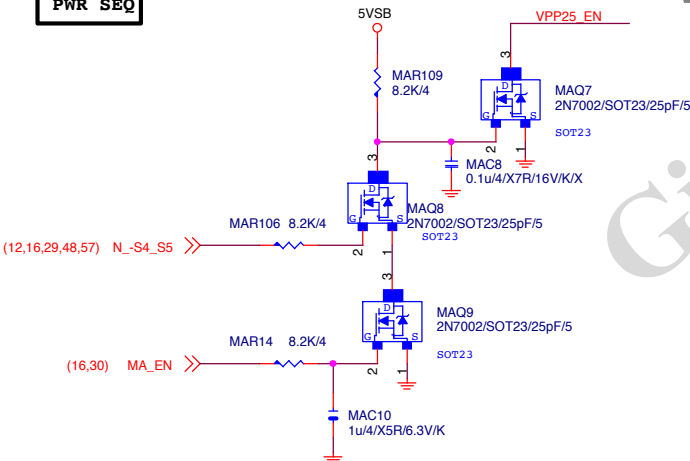
25A MAX

Remote sense請從最重的負載端點拉回

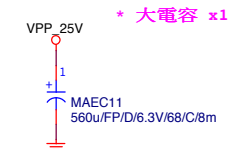
www.aitech1.ru

PWR_SEQ

* 刪 MA_DR32



VPP CAP 560u*1PCS

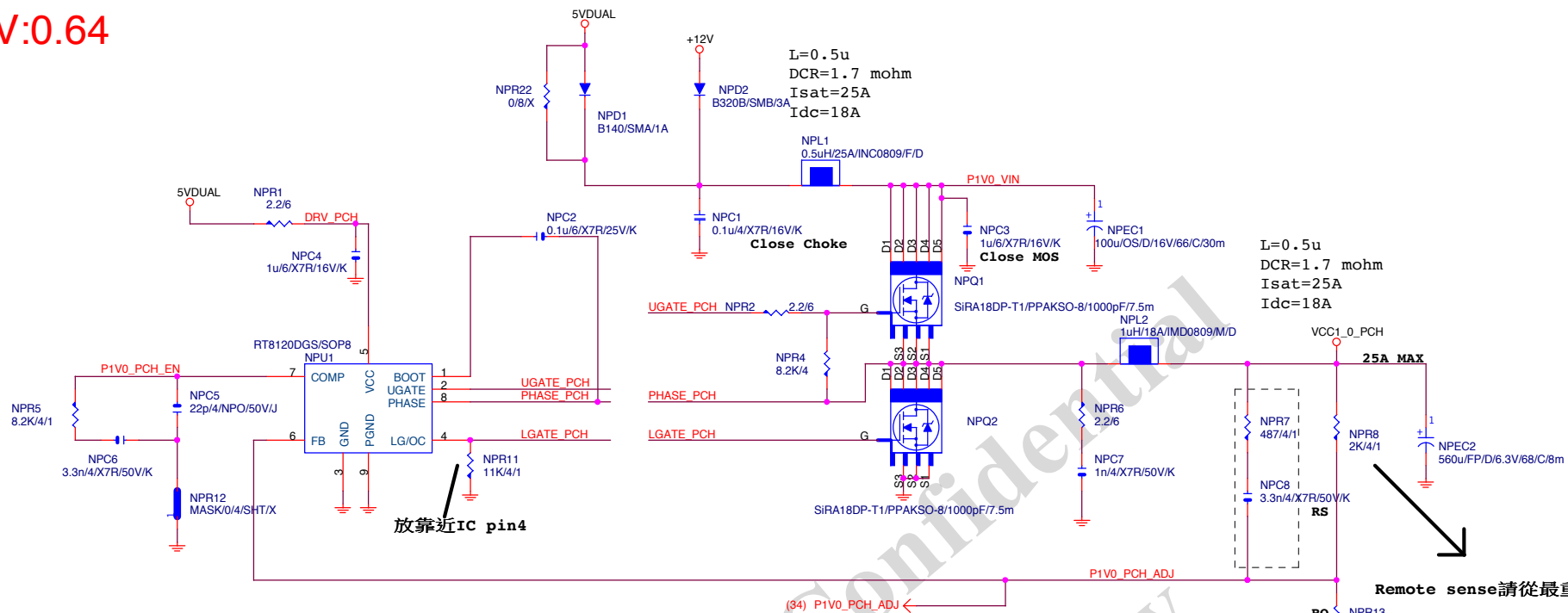


* 大電容 x1

GIGABYTE™

Title		
RT8120_VPP25 POWER		
Size	Document Number	Rev
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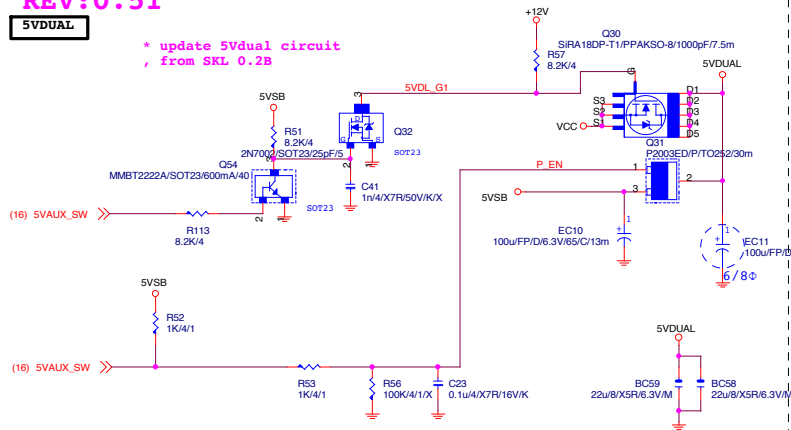
REV:0.64



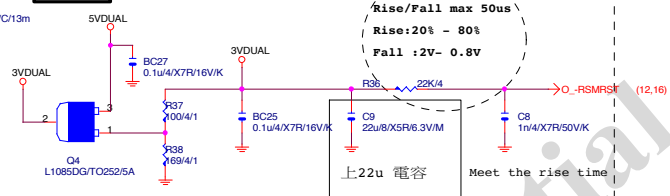
REV:0.51

5VDUAL

* update 5Vdual circuit
from SKL 0.2B



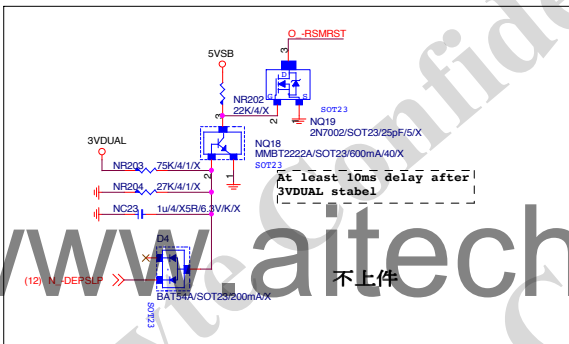
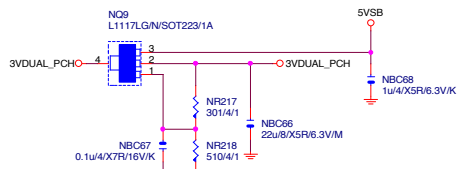
3VDUAL



Rise/Fall max 50us
Rise:20% - 80%
Fall :2V- 0.8V

上22u 电容
Meet the rise time

3VDUAL_PCH



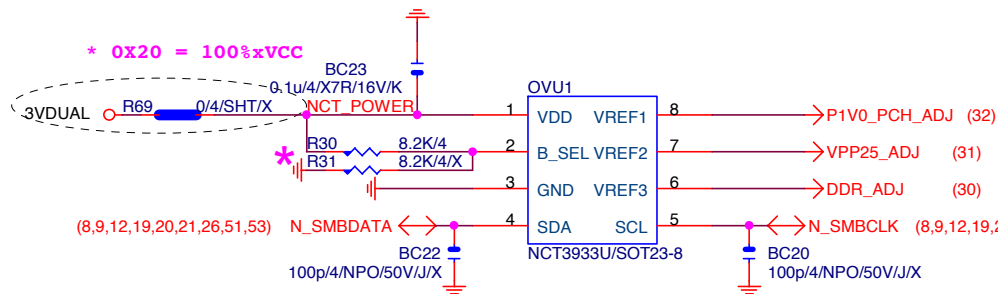
At least 10ms delay after
3VDUAL stable

不上件

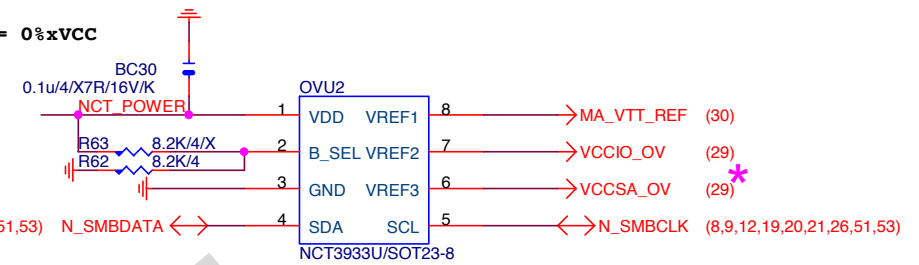
Gigabyte Technology

Title		
DISCRETE POWER		
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OVER VOLTAGE



0X2A = 0%xVCC



0X22 = 75%xVCC

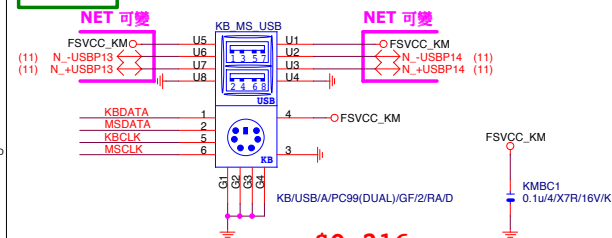
* 删除 OVU3

NCT3933	0X2A	0X20	0X22
VREF1	DDRVTT	VREF_DDRA_DQ	PCH Core
VREF2	VREF_DDRA_CA	N/A	VCC1_5_PCH
VREF3	VREF_DDRA_CA	VREF_DDRB_DQ	SMREF

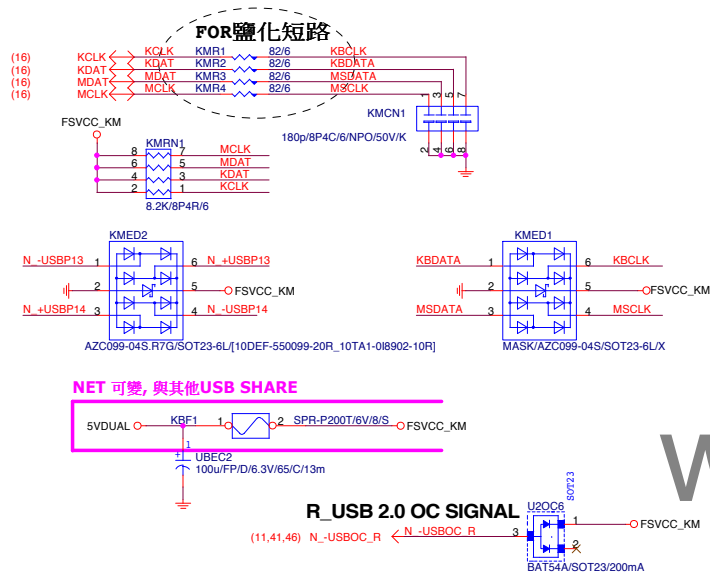
Gigabyte Technology		
Title		
CPU CORE VR-2		
Size	Document Number	Rev
Custom	GA-Z170X-UD3	1.0
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Patch some PSU no internal
pull up resistor





\$0.216



R_USB 2.0 OC SIGNAL

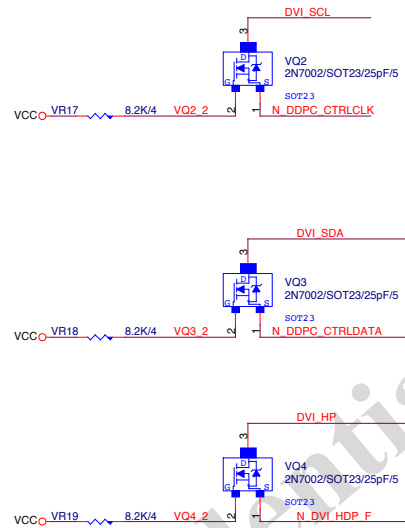
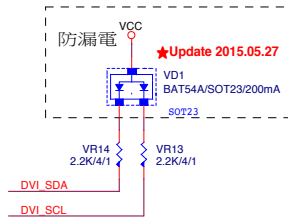
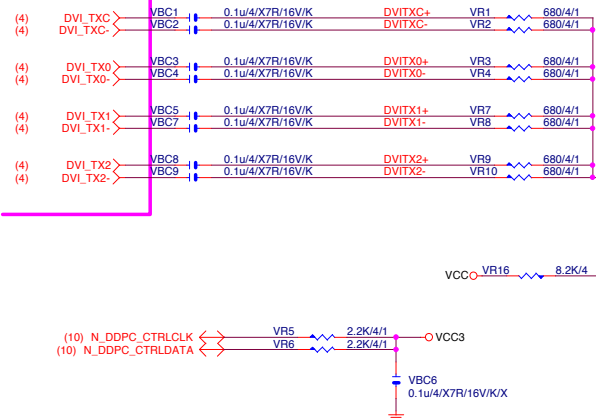
(11,41,46) N-USBOC_R ← N-USBOC_R 3

Rev: 0.7

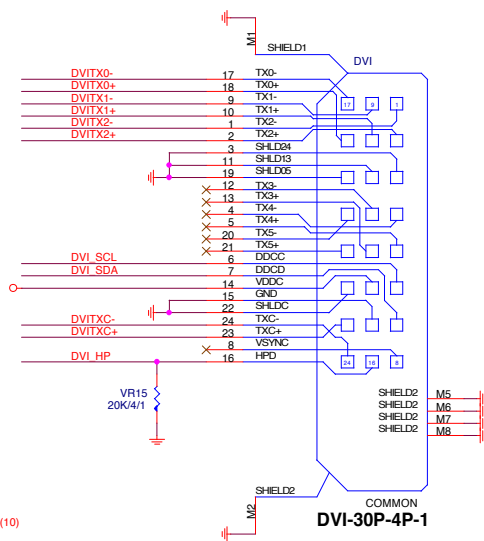
DVI CONN

DVI:20/4/6/4/20
Impedance=85 \pm 17.5%

NET 可變

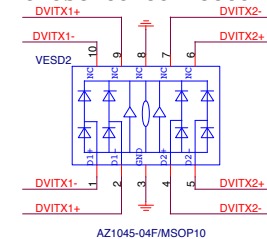


* FSVCC_KM

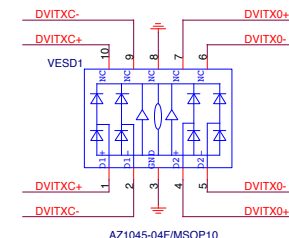


DVI-D/24P/SC/RA/D/SH[11NR6-501024-31R]

Close to connector

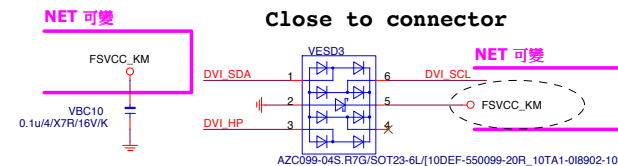


AZ1045-04F/MSOP10



AZ1045-04F/MSOP10

Close to connector



AZC099-04S.R7G/SOT23-6L[U10DEF-550099-20R_10TA1-018902-10R]

Gigabyte Technology

Title			FP,F_USB,USB PWR,BZ
Size			GA-Z170X-UD3
Date:			Monday, July 06, 2015
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省X'TAL COST DOWN:

1. 上件:

DVC28 [10p/4/NPO/50V/J]

DVC11 [10p/4/NPO/50V/J]~修改值

DVR10 [8.2K/4]

2. 删除:

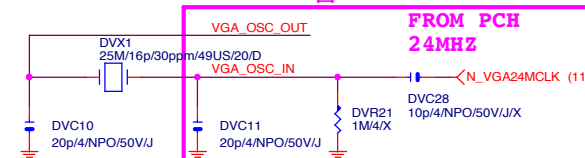
DVX1 [25M/16p/30ppm/49US/20/D]

DVC10 [20p/4/NPO/50V/J]

DVR9 [8.2K/4]

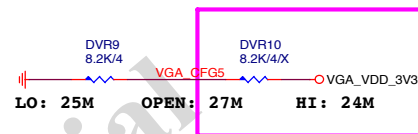
25M Crystal

省X'TAL COST DOWN

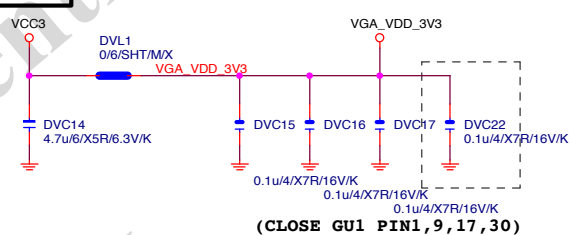


CFG5

For Crystal Less



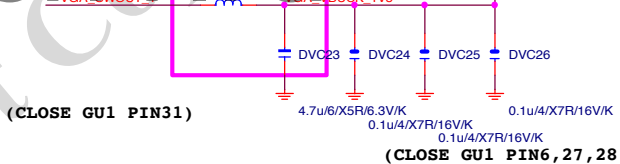
ADAPTER POWER



(CLOSE GU1 PIN1,9,17,30)

LDO MODE: DVL2, DVC23-->X
S.W MODE: DVL2, DVC23-->X

SW MODE

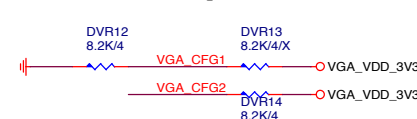


(CLOSE GU1 PIN31)

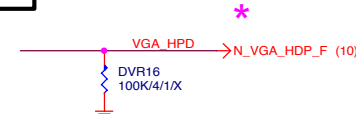
(CLOSE GU1 PIN6,27,28)

CFG1&2

Non-Compliant

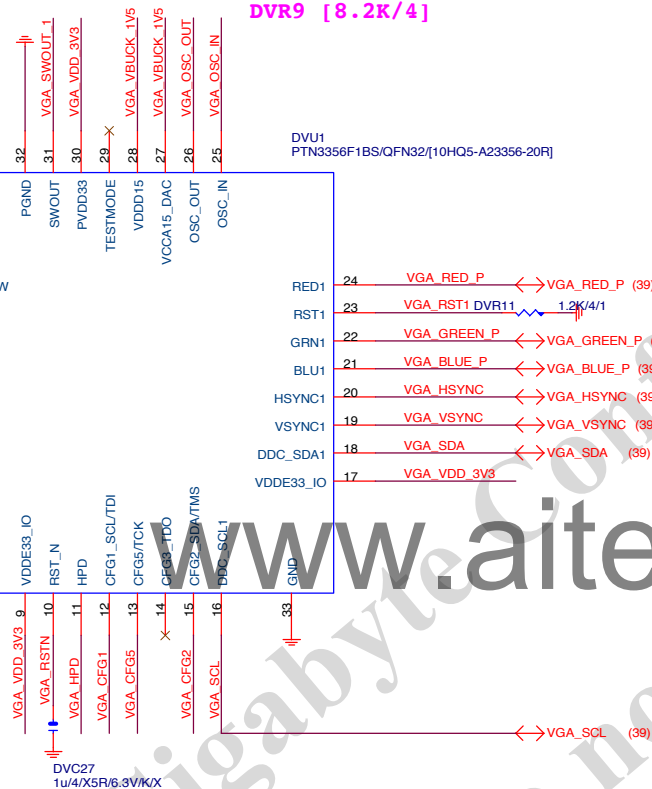


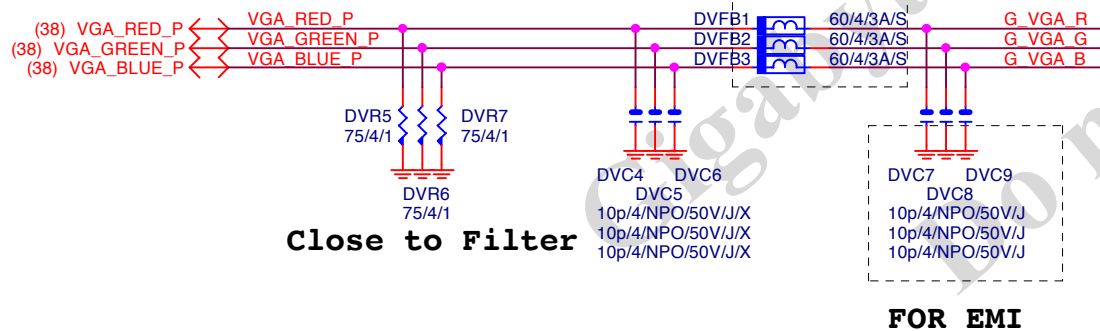
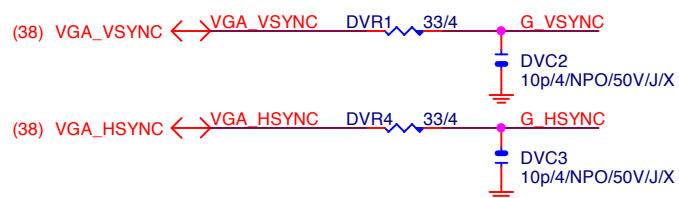
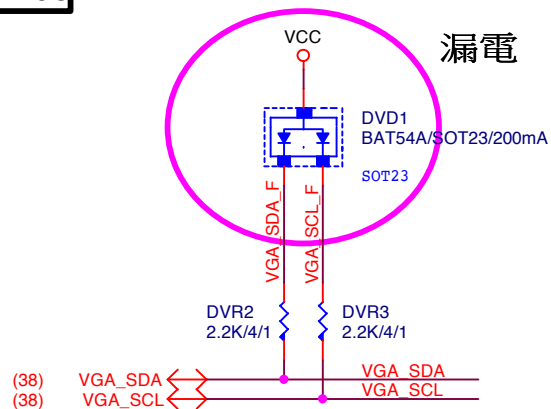
HPD

Gigabyte Technology
NXP-PTN3356

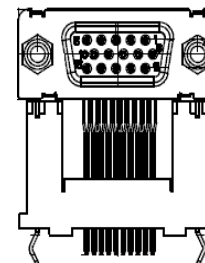
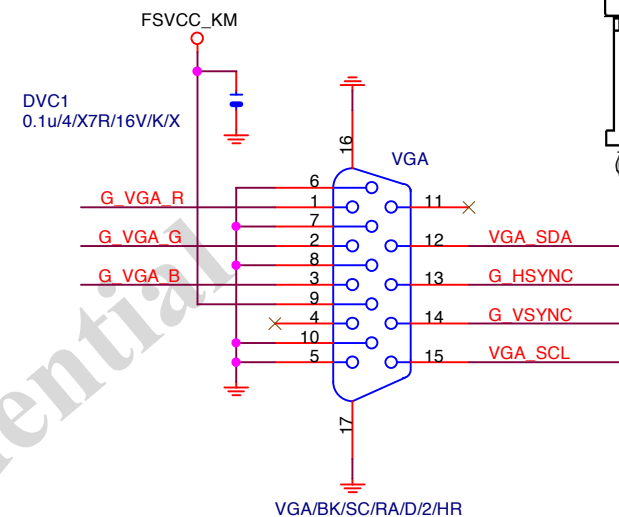
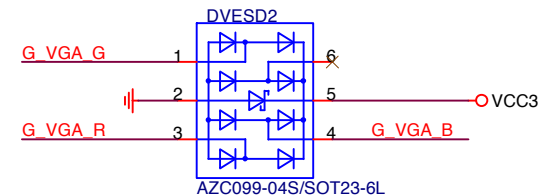
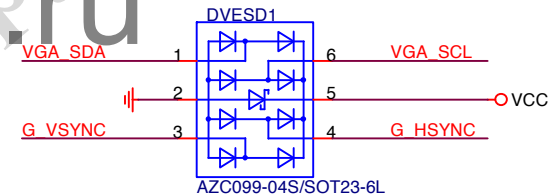
Title	GA-Z170X-UD3	Rev	1.0
Size	Document Number		
Custom			
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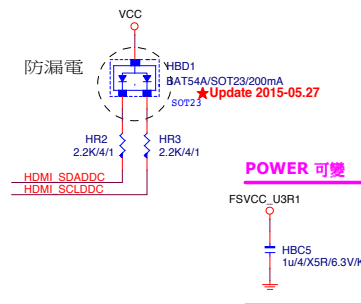
放置PCH端





VGA CONN. 架高型VGA (BLACK)

**VGA ESD**

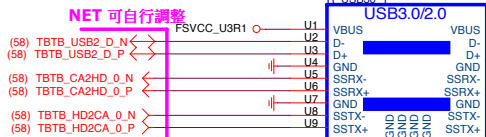


【技術通報R&D技術通報150】
HDMI eye diagram.4版(deep color)會fail
原因: 因目前的HDMI訊號過長,造成RISING TIME過慢,而會壓到eye diagram
改善: ASMEDIA ASM1442 : 3.16K(PIN6 PULL DOWN電阻) 10ohm(PIN4 PULL DOWN電阻)

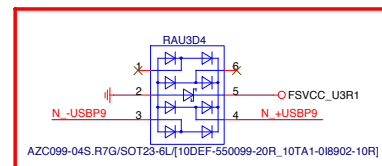
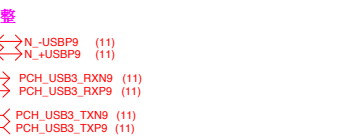
Rev: 0.7

R_USB30_1

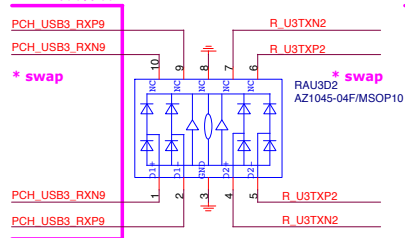
NET 可自行調整



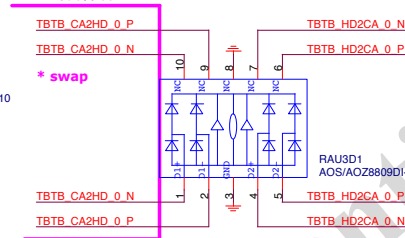
NET 可自行調整



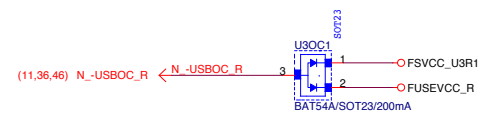
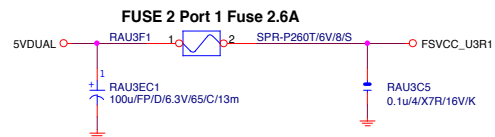
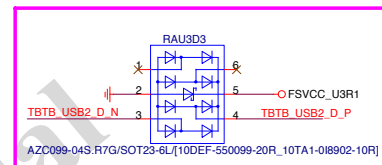
NET 可自行調整



NET 可自行調整



NET 可自行調整

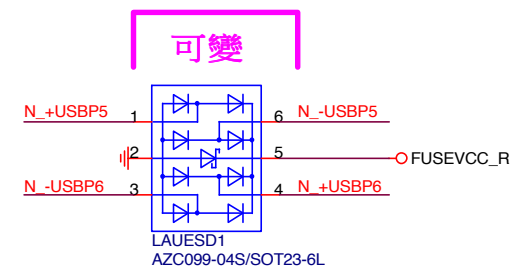


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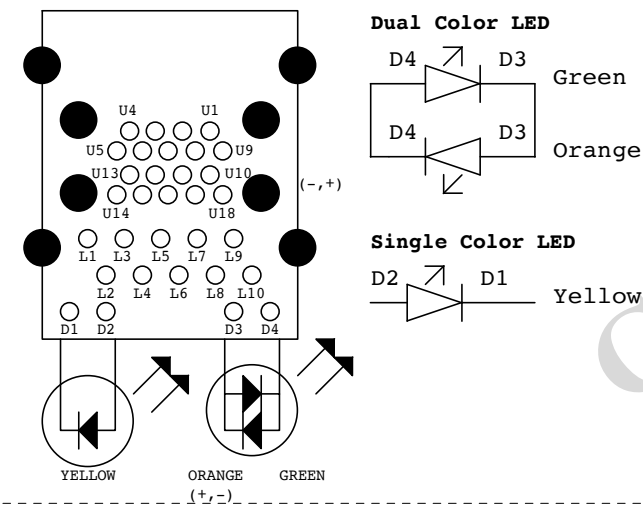
Gigabyte Technology			
Title R_USB30,F_USB30, USB OC			
Size	Document Number	GA-Z170X-UD3	
Custom		Rev 1.0	
Date:	Monday, July 06, 2015	Sheet	41 of 60

USB_LAN CONNECTOR R1.09

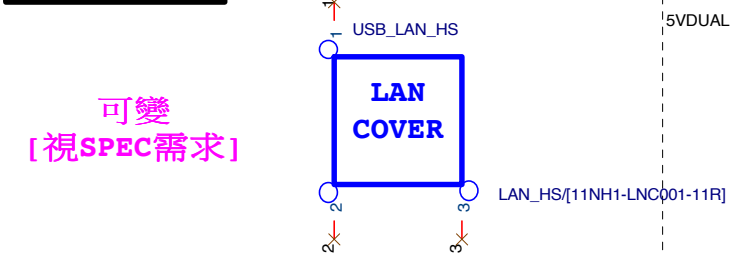
RMA ESD PROTECT note:可變更USB NAME



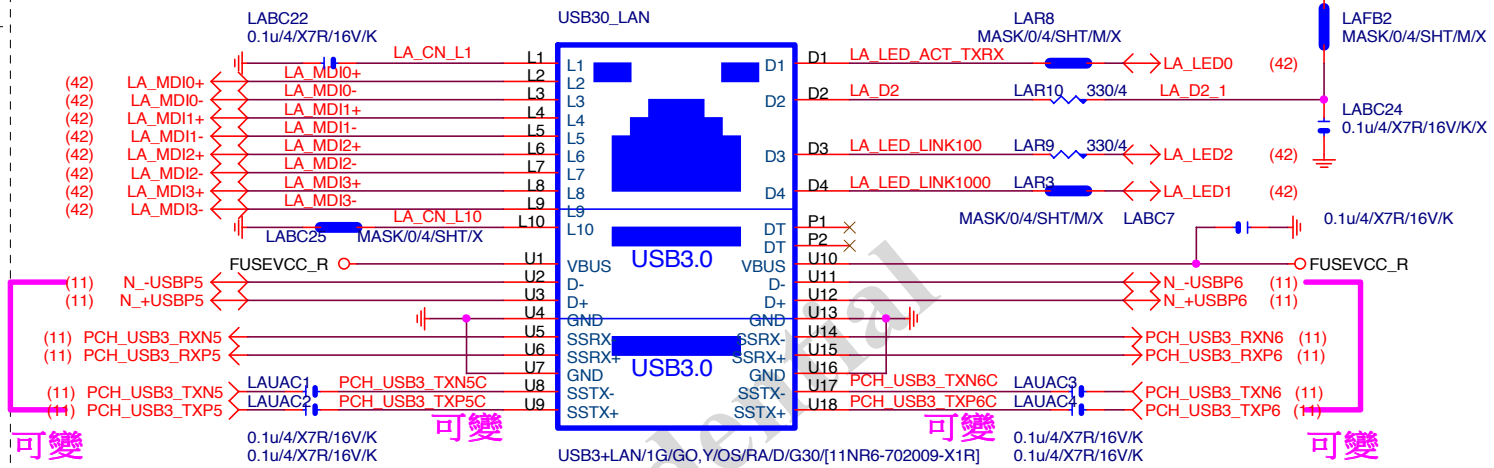
USB30_LAN LAYOUT示意圖



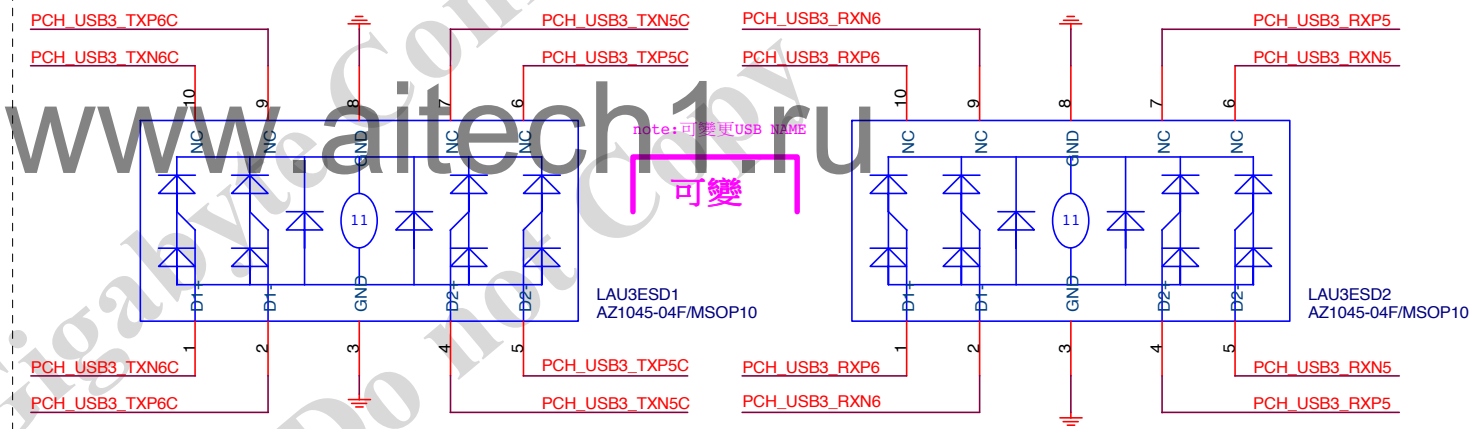
LAN_COVER FOOT PRINT:LAN_COVER



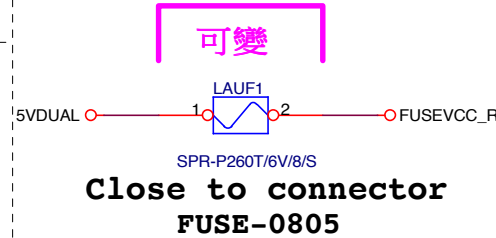
USB_LAN CONNECTOR [I219] note:可變更USB NAME



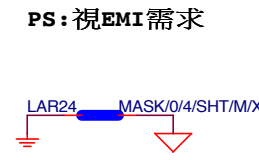
LA_MDI--->100歐姆:[20/4/8/4/20]



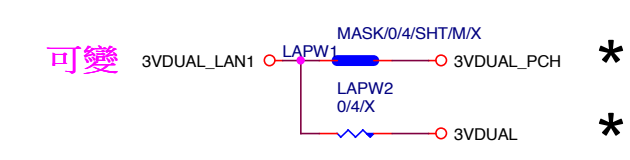
USB POWER note:可變更FUSE



EMI SHORT PAD PS:視EMI需求



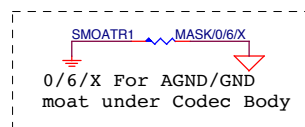
LAN POWER note:lan power連接及電流



Gigabyte Technology		
LAN CONNECTOR-I219		
Size	Document Number	Rev
Custom	GA-Z170X-UD3	1.0
Date:	Monday, July 06, 2015	Sheet 43 of 60

**ALC1150 五孔+SPDIF
AUDIO JACK**

<input type="radio"/> MH1 DGND	MH2 <input type="radio"/> Isolate	
---	--	--



Analog Area

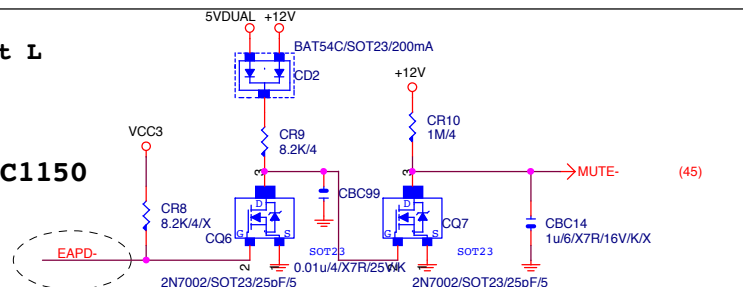
Thermal pad is DGND

Digital Area

(45)	FRONT_JD	CR18	10K/4/1
(45)	LINE1_JD	CR39	20K/4/1
(45)	MIC1_JD	CR16	39.2K/4/1
(45)	SURR_JD	CR48	10K/4/1
(45)	CEN_JD	CR40	39.2K/4/1
JD resistors close CODEC			
(45)	FAUDIO_JD	CR28	47/4/1

```
EAPD: Default L
H : ON
L : OFF
```

Close to ALC1150



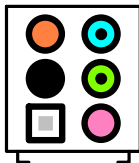
**LAYOUT注意:要加
GND切割線**

音效區域印刷

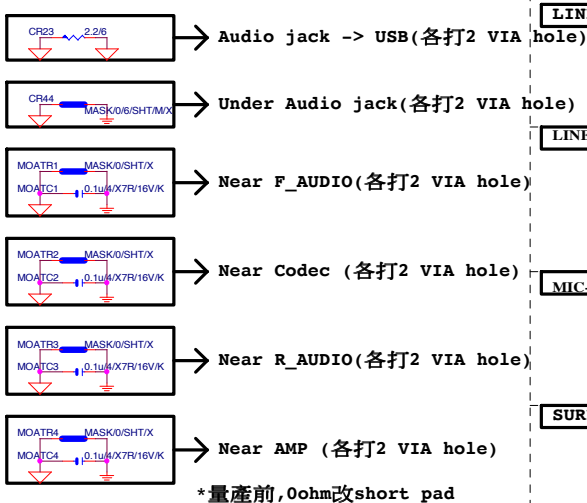
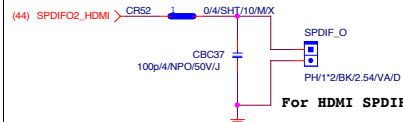
Gigabyte Technology

Title			
ALC1150			
Size Custom	Document Number		Rev
	GA-Z170X-UD3		1.0
Date:	Monday, July 06, 2015	Sheet	44 of 60

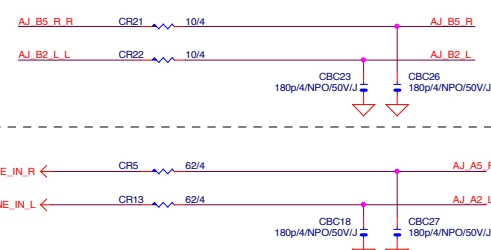
AZALIA JACK



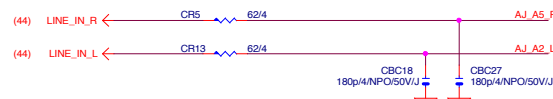
SPDIF_OUT



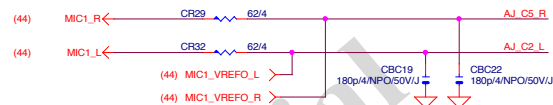
LINE-OUT



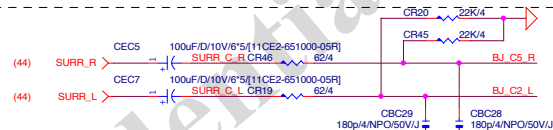
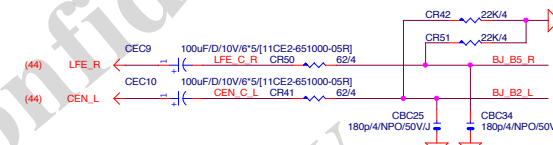
LINE-IN



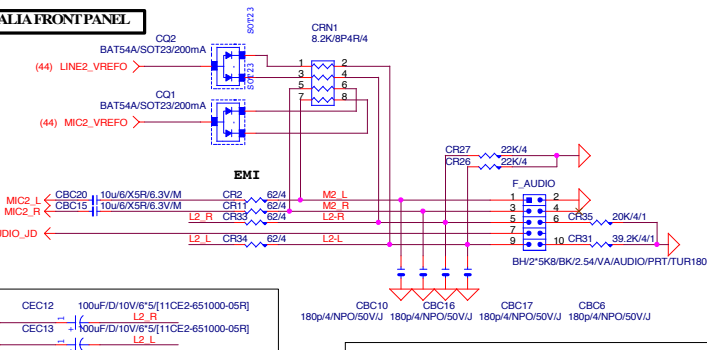
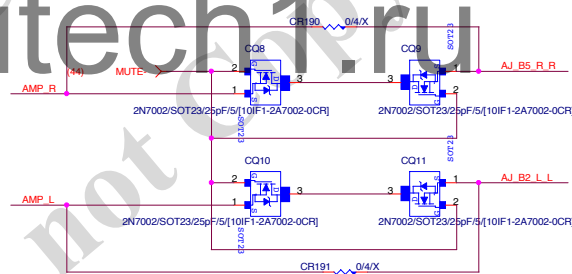
MIC-IN



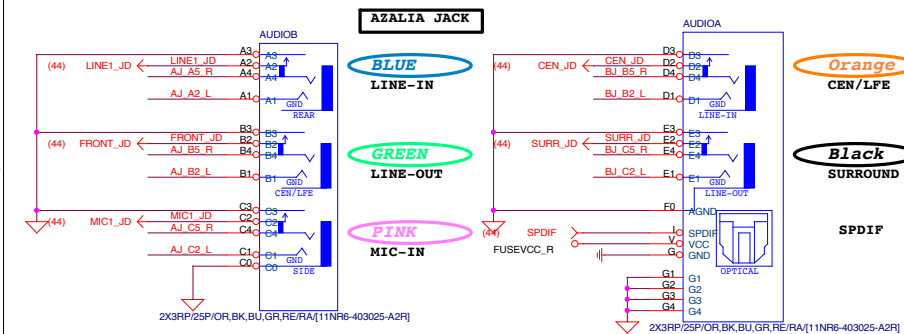
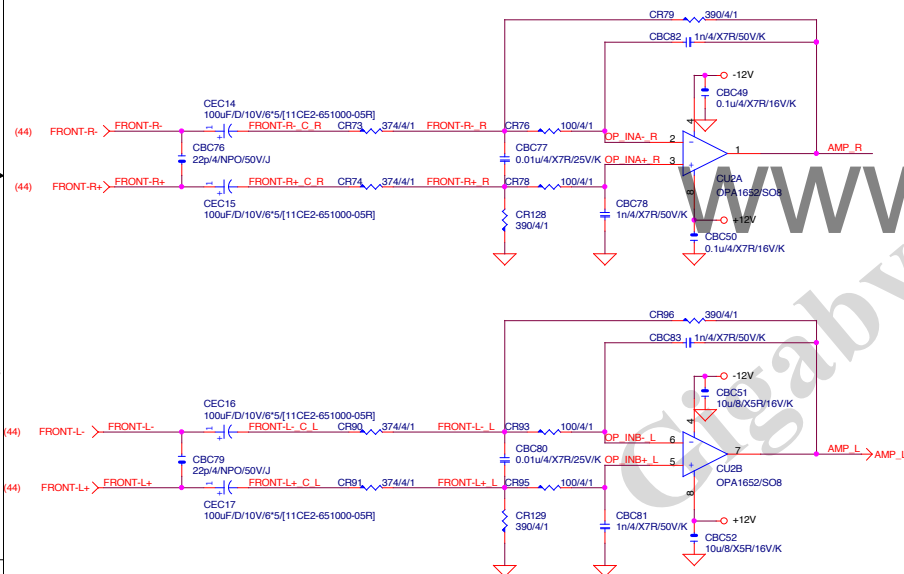
SURROUND

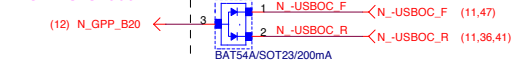
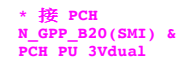
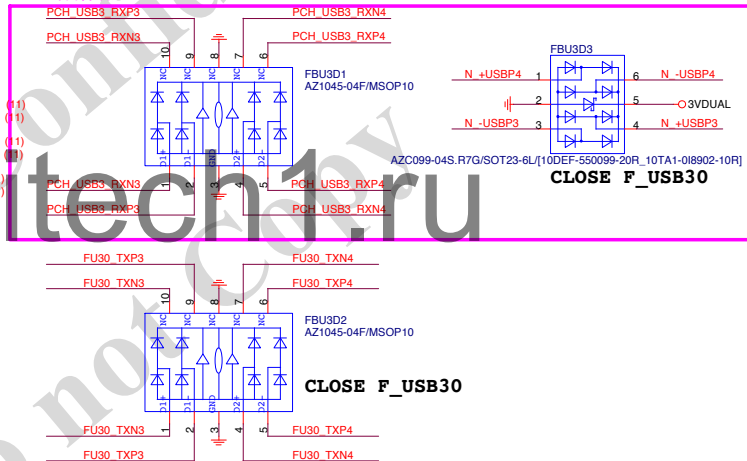
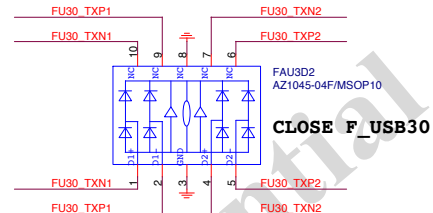
**CEN/LFE**

AZALIA FRONT PANEL

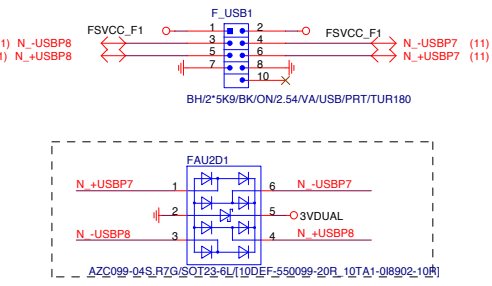


Differential to Single-End AMPLIFIED

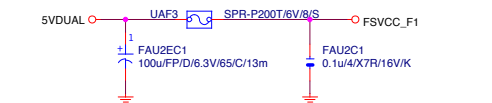




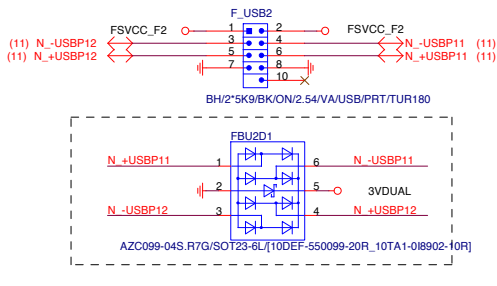
NET 可變



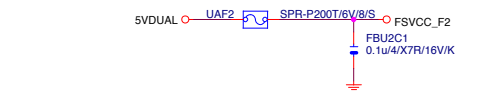
Close to connector
FUSE 2 Port 1 Fuse 2A



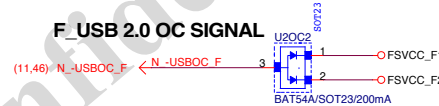
NET 可變



Close to connector
FUSE 2 Port 1 Fuse 2A

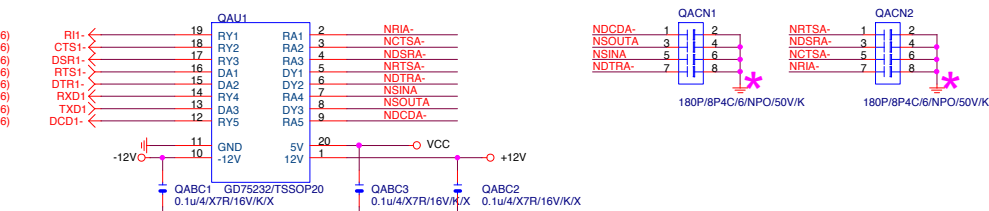


F_USB 2.0 OC SIGNAL

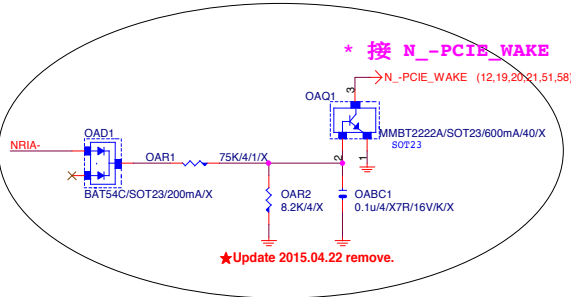
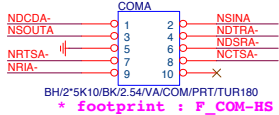


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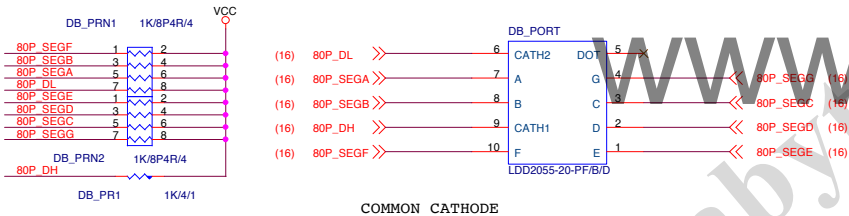
COM PORT



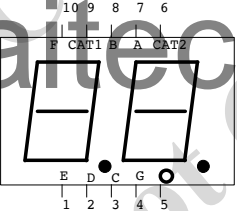
COMA



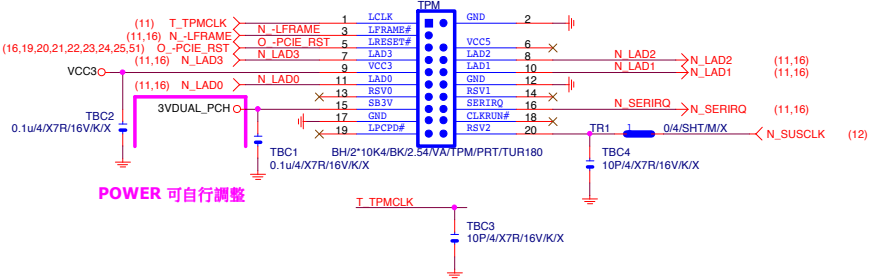
80 PORT



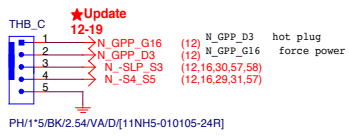
Physical Package (TOP VIEW)



TPM CONNECT



Thunderbolt

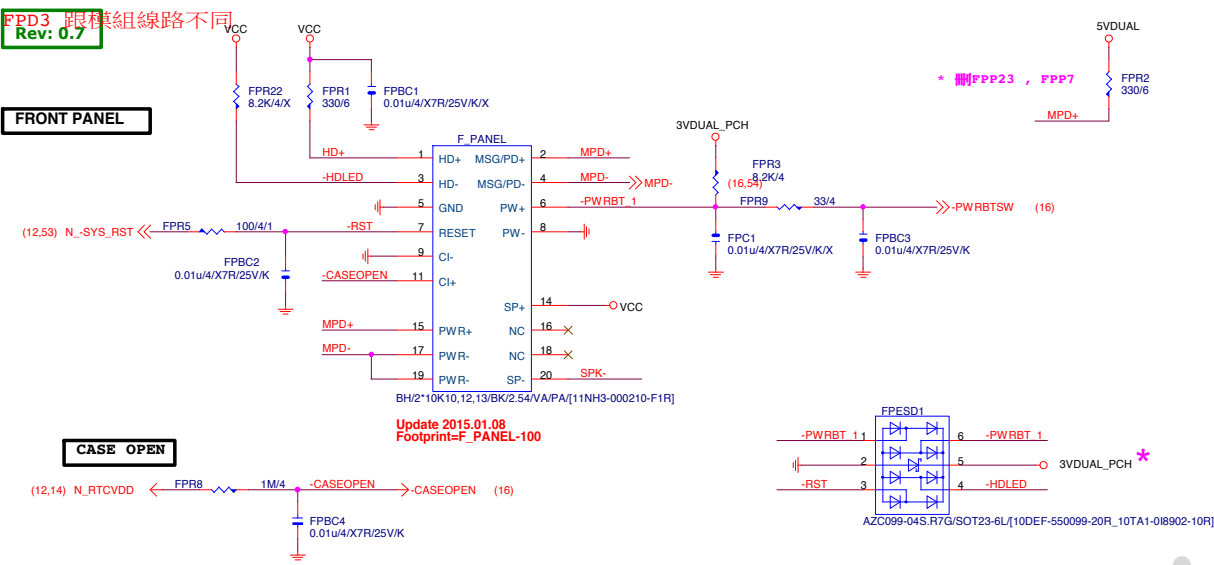


Gigabyte Technology

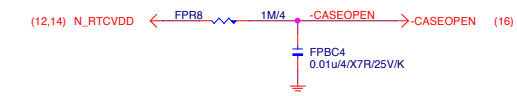
Title			FP,F_USB,USB PWR,BZ
Size	Document Number	GA-Z170X-UD3	
Custom		Rev	1.0
Date:	Monday, July 06, 2015	Sheet	48 of 60

FDP3 跟模組線路不同
Rev: 0.7

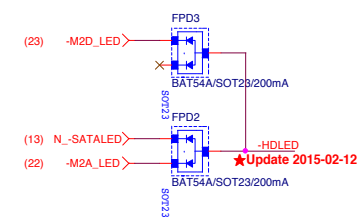
FRONT PANEL



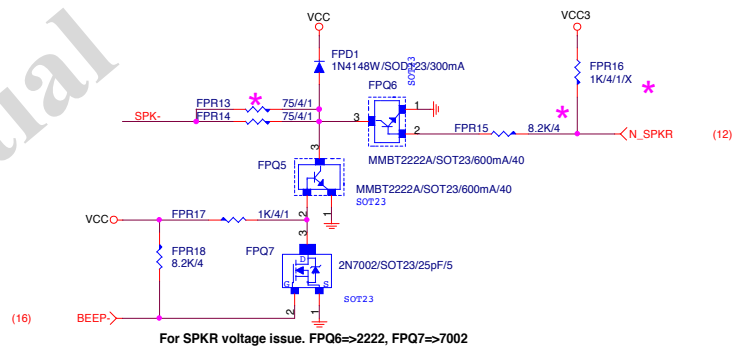
CASE OPEN



SATA LED



SPKR



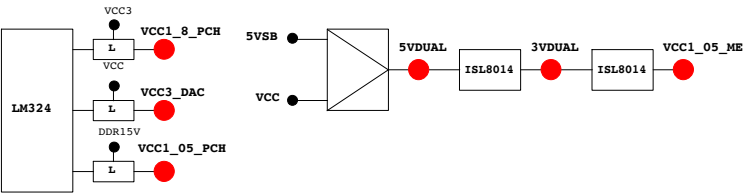
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PCH GPIO LIST TABLE					
PIN NAME	PWR	Default	USAGE	NOTE	
GP0	MAIN	H-Z	GPI	GPIO0	N/A
GP1/TACH1	MAIN		GPI	GPIO1	N/A
GP2/PIRQE#	MAIN		GPI	-PIRQE	P/U 8.2K VCC3
GP3/PIRQF#	MAIN		GPI	-PIRQF	P/U 8.2K VCC3
GP4/PIRQG#	MAIN		GPI	-PIRQG	P/U 8.2K VCC3
GP5/PIRQH#	MAIN		GPI	-PIRQH	P/U 8.2K VCC3
GP6/TACH2	MAIN		GPI	PCIEX1 Detect	P/U 8.2K VCC3
GP7/TACH3	MAIN		GPI	GPIO7	P/U 8.2K VCC3
GP8	STBY	H	GPI	GPIO8	N/A
GP9/OC5#	STBY		NATIVE	USB OC5#	N/A
GP10/OC6#	STBY		NATIVE	USB OC6#	N/A
GP11/SMBALERT#	STBY		NATIVE	USB PWR protect	P/U 8.2K 3VDUAL
GP12	STBY	L	GPI	GPIO12	N/A
GP13	STBY	L	GPI	LPCPME#	P/U 8.2K 3VDUAL
GP14/OC7#	STBY		NATIVE	USB OC7#	N/A
GP15	STBY	L	GPI	GPIO15(TLS Enable)	P/U 8.2K 3VDUAL
GP16	MAIN		GPI	GPIO16	P/U 8.2K VCC3
GP17/TACH0	MAIN		GPI	GPIO17	P/U 8.2K VCC3
GP18	MAIN		GPI	Mobile Only	N/A
GP19	MAIN		GPI	GPIO19	P/U 8.2K VCC3
GP20	MAIN		GPI	GPIO20	P/U 8.2K VCC3
GP21	MAIN		GPI	GPIO21	P/U 8.2K VCC3
GP22	MAIN	H-Z	GPI	GPIO22	P/U 8.2K VCC3
GP23	MAIN		GPI	GPIO23	N/A
GP24	STBY	L	GPI	SKTOCC#	N/A
GP25	STBY			Mobile Only	N/A
GP26	STBY			Mobile Only	N/A
GP27	STBY	H	GPO	GPIO27	P/U 8.2K 3VDUAL
GP28	STBY	H	GPO	PWR LED	P/U 8.2K 3VDUAL
GP29	STBY	L	GPI	GPIO29	N/A
GP30	STBY	H-Z	GPI	Mobile Only	N/A
GP31	STBY	H-Z	GPI	Mobile Only	N/A
GP32	MAIN	H	GPO	N/A	N/A
GP33	MAIN	H	GPO	N/A	N/A
GP34	MAIN	H-Z	GPI	-PCI_STOP	P/U 8.2K VCC3
GP35	MAIN	L	GPO	-ACZ_DET	P/U 8.2K VCC3
GP36	MAIN		GPI	N/A	N/A
GP37	MAIN		GPI	N/A	N/A
GP38	MAIN	H-Z	GPI	PCIEX4 Detect	P/U 8.2K VCC3
GP39	MAIN	H-Z	GPI	GPIO39	P/U 8.2K VCC3
GP40	STBY		NATIVE	USB OC1#	N/A
GP41	STBY		NATIVE	USB OC2#	N/A
GP42	STBY		NATIVE	USB OC3#	N/A
GP43	STBY		NATIVE	USB OC4#	N/A
GP44	STBY	L	NATIVE	GPIO44	P/U 8.2K 3VDUAL
GP45	STBY		NATIVE	GPIO45	P/U 8.2K 3VDUAL
GP46	STBY	L	NATIVE	GPIO46	P/U 8.2K 3VDUAL
GP47	STBY			Mobile Only	N/A
GP48	MAIN	H-Z	IN	GPIO48	P/U 8.2K 3VDUAL
GP49	MAIN	H-Z	IN	GPIO49	P/U 8.2K 3VDUAL
GP50	MAIN		NATIVE	-REQ1	P/U 2.2K VCC
GP51	MAIN	H	NATIVE	-GNT1	N/A
GP52	MAIN		NATIVE	-REQ2	P/U 2.2K VCC
GP53	MAIN	H	NATIVE	-GNT2	N/A
GP54	MAIN		NATIVE	-REQ3	P/U 2.2K VCC
GP55	MAIN	H	NATIVE	-GNT3	N/A
GP56	STBY		NATIVE	Mobile Only	N/A
GP57	STBY	H-Z	IN	VCORE_OV1	P/U 8.2K 3VDUAL
GP58	STBY	H-Z	NATIVE	F_USB_OC	P/U 8.2K 3VDUAL
GP59	STBY		NATIVE	USB_OC0#	N/A
GP60	STBY	H-Z	NATIVE	N/A(Reverse)	P/U 8.2K 3VDUAL
GP61	STBY	L	NATIVE	-SUSTAT	N/A
GP62	STBY	L	NATIVE	SUSCLK	N/A
GP63	STBY	L	NATIVE	GPIO63	N/A
GP64	MAIN	L	NATIVE	CLKOUTFLEX0	N/A
GP65	MAIN	L	NATIVE	CLKOUTFLEX1	N/A
GP66	MAIN	L	NATIVE	CLKOUTFLEX2	N/A
GP67	MAIN	L	NATIVE	CLKOUTFLEX3	N/A
GP72	STBY	H-Z	NATIVE	VCORE_OV4	P/U 8.2K 3VDUAL
GP73	STBY			Mobile Only	N/A
GP74	STBY	H-Z	NATIVE	1_05V_OV2	P/U 8.2K 3VDUAL
GP75	STBY	H-Z	NATIVE	N/A(Reverse)	P/U 8.2K 3VDUAL

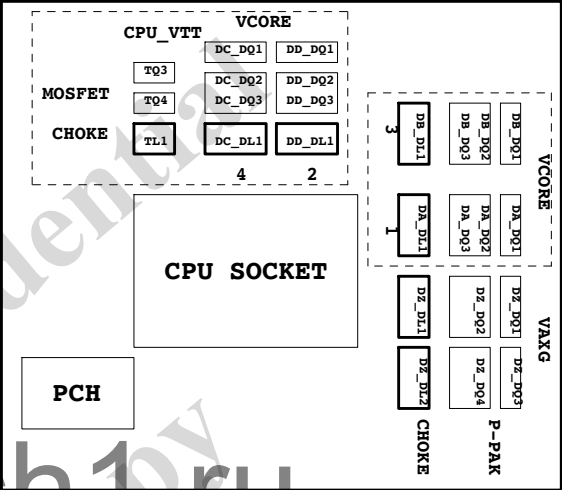
Super I/O ITE8720 GPIO Table

PIN NAME	USAGE	NOTE
SVC/PECI_RQT/GP14	-PECI_REQ	
PWROK1/GP13	PWROK1/ITE_PWROK	
KRST#/GP62	-KBRST	
SO/GP50	-ICH_SPI_CS	
IRTX/GP47/CE2_N/JP7	CEB_N	
GP46/IRRX	-LAN2_DSM	
PSION#/GP42	-PSON	
PWROK2#/GP41	PECI_CTL	
PCIRST3#/GP10/VDIMM_STR_EN	-PCIE_RST	
RSMRST#CIRRXL/GP55	-RSMRST	
PME#/GP54	-LPCPME	
PD5/GP75/BUSS00	N/A	

PIN NAME	USAGE	NOTE
FAN_TAC2/GP52	FANIO2	
FAN_TAC3/GP37	FANIO3	
VIDO3/FAN_TAC4/GP25/DSR2#	FANIO4	
FAN_CTL2/GP51	FANPWM2	
FAN_CTL3/GP36	FANPWM3	
VID4/GP34	BEEP-	
VID3/GP33	TURBO1	
VID2/GP32	TURBO0	
VCORE_GOOD/VID6/GP63	CPUT_LED1_C	
VID5/GP35	CPUT_LED2_C	
VID1/GP31	CPUT_LED3_C	
VID0/GP30	-LAN1_DSM	NBT_LED1_C
SLCT/GP80	CPU_LED1_C	
PE/GP81	CPU_LED2_C	
BUSY/GP82	CPU_LED3_C	
PD3/GP73/BUSSI1	SB_LED1_C	
PD4/GP74/BUSSI2	SB_LED2_C	
VCORE_EN/VID7/GP64	IT_GP64	SB_LED3_C
PD0/GP70	NB_LED1_C	
PD1/GP71	NB_LED2_C	
PD2/GP72/BUSSI0	NB_LED3_C	
GP22/SCK	LOW_PWR_1	
VID05/GP27/SIN2	LOW_PWR_2	
PCIRST2#/GP11	-PWRST1	
PCIRST1#/GP12	-PWRST2	
3VBSW#/GP40	CSI_F0	BSEL166_1
SUSC#/GP53	CSI_F1	BSEL166_2
GP23/SI	BSEL166_3/CSISBSL	
VID00/GP20/CTS2#	CPUT_LED1_C	BSEL166_4
GP65/VDDA_EN/GB_01	MB_ID2	
PD6/GP76/BUSS01	MB_ID3	
PD7/GP77/BUSS02	MB_ID4	
AFD#/GP86/SMB_C_R	3V PIN	FST_2X8
INIT#/GP85/SMB_D_M	SEC_2x8	GTLREF_AD2
ACK#/GP83	DDR_LED1_C	
VID01/GP21/DCD2#	DDR_LED2_C	
STB#/GP87/SMB_C_M	DDR_LED3_C	
PWRON#/GP44	VCORE_OV1	
PANSW#/GP43	PWRBTSW	
KDAT/GP61	-PWRBTSW	
KCLK/GP60	KDAT	
MDAT/GP57	KCLK	
MACL/GP56	MDAT	
GP66/VLDT_EN/GB_02	NBT_LED1_C	MCLK
SVD/PCIRSTIN#/CIRTX/GP15	PWM2_CR	
KDAT/GP61	PWM2_CR	
GP67/CPU_PG/GB_03	EN_LOADLINE	IT_GP67/-EN_PWM2
SLIN#/GP84/SMB_D_R	-EN_PWM2	
PSI_L/FAN_CLT5/CIRRXL2/GP16	-THERM	
VID04/GP26/SOUT2	DDR18V_PH2_EN	
VID02/FAN_TAC5/GP24/DSR2#	DDR18V_LED	
VID06/GP17/RI2#	1_1V_PH_EN	
VID07/JP6/DTR2#	JP6	
PD5/GP75/BUSS00	SB_LED3_C	



PWM各相位的擺法如下：



BIOS超電壓對應表：

線路圖名稱	BIOS選項
Vcore	CPU Vcore
CPU_VTT	CPU Termination
CPU_VAXG	CPU Graphic Core
VCC1_8_PCH	CPU PLL
VCC1_05_PCH	PCH core
3VDUAL	3VDUAL
DDR15V	DRAM voltage
DDRVTT	DRAM Terminatio
VREF_CA_A/VREF_CA_B	DRAM Address Ref
VREF_DQ_A/VREF_DQ_B	DRAM Data Ref

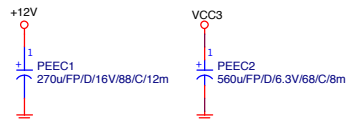
散熱模組料號：

Z77-D3H :
PCH :
12SP2-S05511-01R/02R/03R
MOSFET :
12SP2-S08924-01R/02R/03R

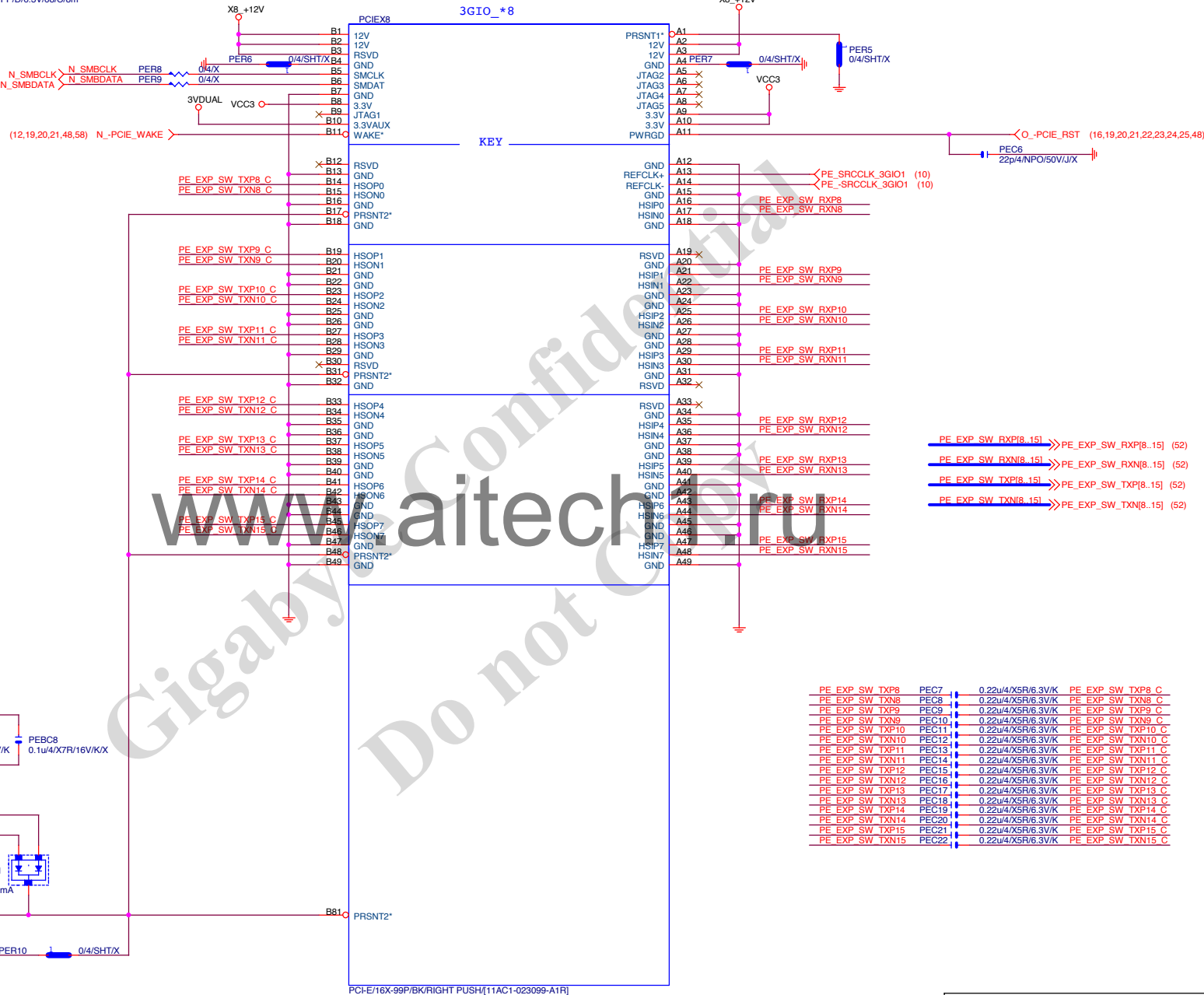
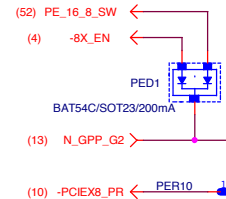
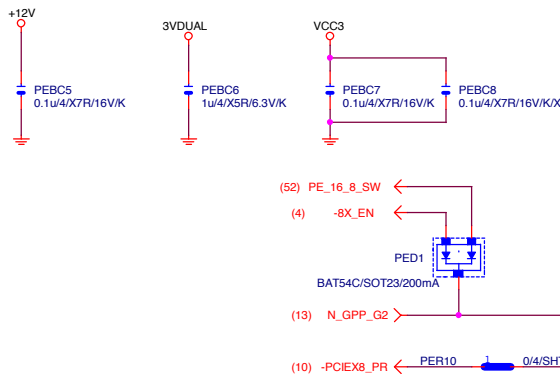
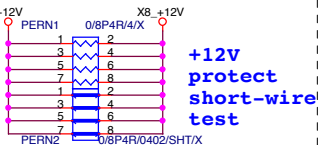
	3 pin FAN control	4 pin FAN control	FAN speed	Controller
CPU FAN	FANPWM1	FANPWM3	FANIO1	IT8720
	ICH_FAN_PWM2	ICH_FAN_PWM0	ICH_FAN_TACH0	PCH
SYS FAN	FANPWM2	N/A	FANIO2	IT8720
	ICH_FAN_PWM1	N/A	ICH_FAN_TACH1	PCH
PWR FAN	N/A	N/A	FANIO3	IT8720
			ICH_FAN_TACH2	PCH

Gigabyte Technology			
Title	TABLE LIST		
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Rev 0.3

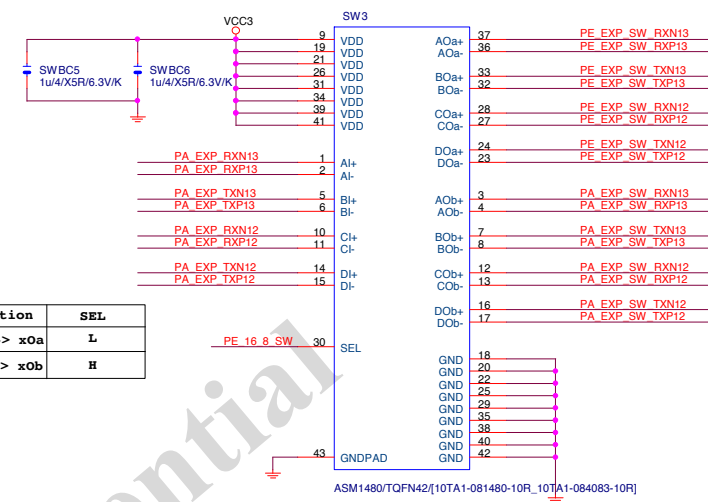
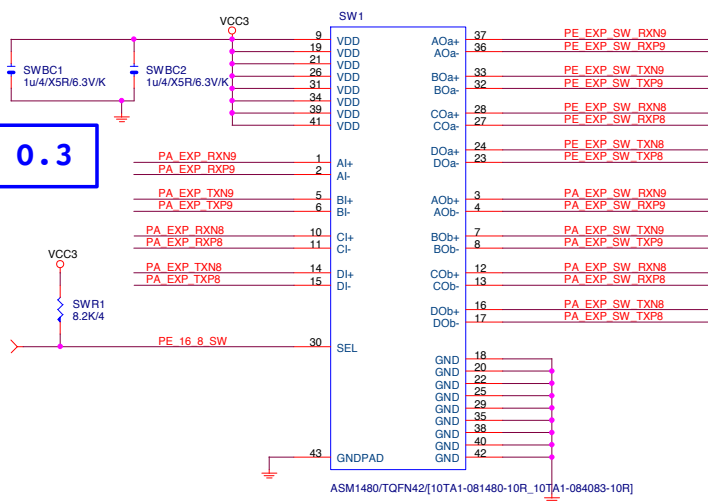


PCIEX8 PROTECT SHT

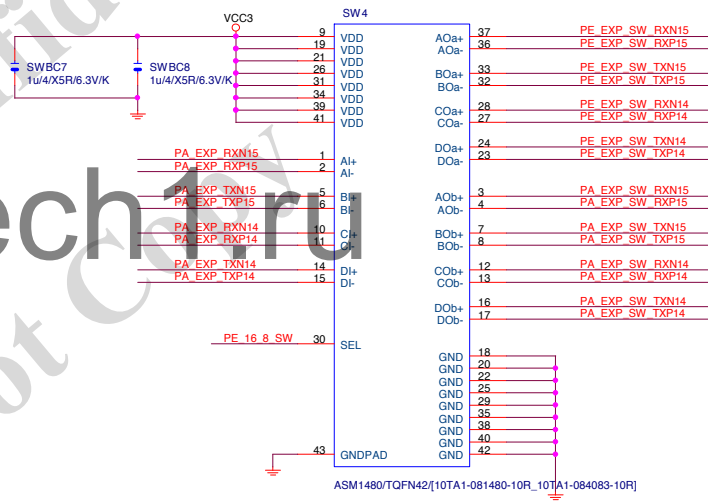
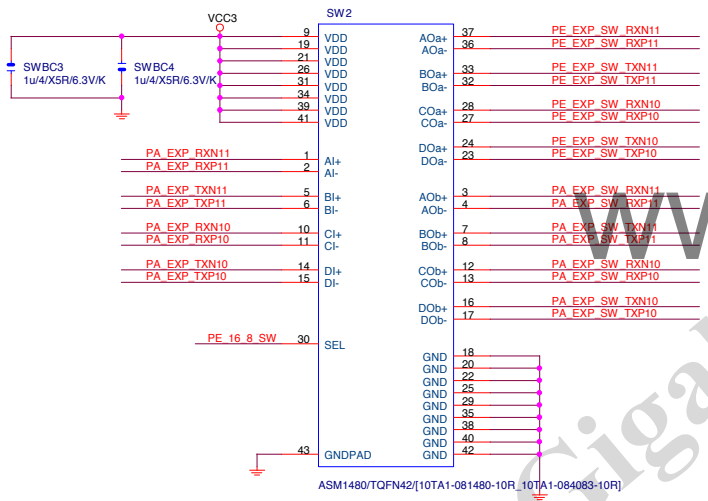


PE EXP SW TXP8	PEC7	0.22u4/X5R/6.3V/K	PE EXP SW TXP8_C
PE EXP SW TXN8	PEC8	0.22u4/X5R/6.3V/K	PE EXP SW TXN8_C
PE EXP SW TXP9	PEC9	0.22u4/X5R/6.3V/K	PE EXP SW TXP9_C
PE EXP SW TXN9	PEC10	0.22u4/X5R/6.3V/K	PE EXP SW TXN9_C
PE EXP SW TXP10	PEC11	0.22u4/X5R/6.3V/K	PE EXP SW TXP10_C
PE EXP SW TXN10	PEC12	0.22u4/X5R/6.3V/K	PE EXP SW TXN10_C
PE EXP SW TXP11	PEC13	0.22u4/X5R/6.3V/K	PE EXP SW TXP11_C
PE EXP SW TXN11	PEC14	0.22u4/X5R/6.3V/K	PE EXP SW TXN11_C
PE EXP SW TXP12	PEC15	0.22u4/X5R/6.3V/K	PE EXP SW TXP12_C
PE EXP SW TXN12	PEC16	0.22u4/X5R/6.3V/K	PE EXP SW TXN12_C
PE EXP SW TXP13	PEC17	0.22u4/X5R/6.3V/K	PE EXP SW TXP13_C
PE EXP SW TXN13	PEC18	0.22u4/X5R/6.3V/K	PE EXP SW TXN13_C
PE EXP SW TXP14	PEC19	0.22u4/X5R/6.3V/K	PE EXP SW TXP14_C
PE EXP SW TXN14	PEC20	0.22u4/X5R/6.3V/K	PE EXP SW TXN14_C
PE EXP SW TXP15	PEC21	0.22u4/X5R/6.3V/K	PE EXP SW TXP15_C
PE EXP SW TXN15	PEC22	0.22u4/X5R/6.3V/K	PE EXP SW TXN15_C


51) PE_16_8_SW :

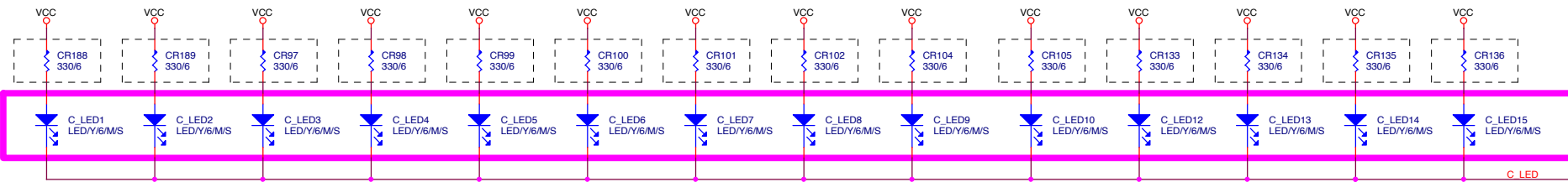


Function	SEL
xI--> xOa	L
xI--> xOb	H



IDT6V41530

			
Title IDT6V41510_CLK BUFFER			
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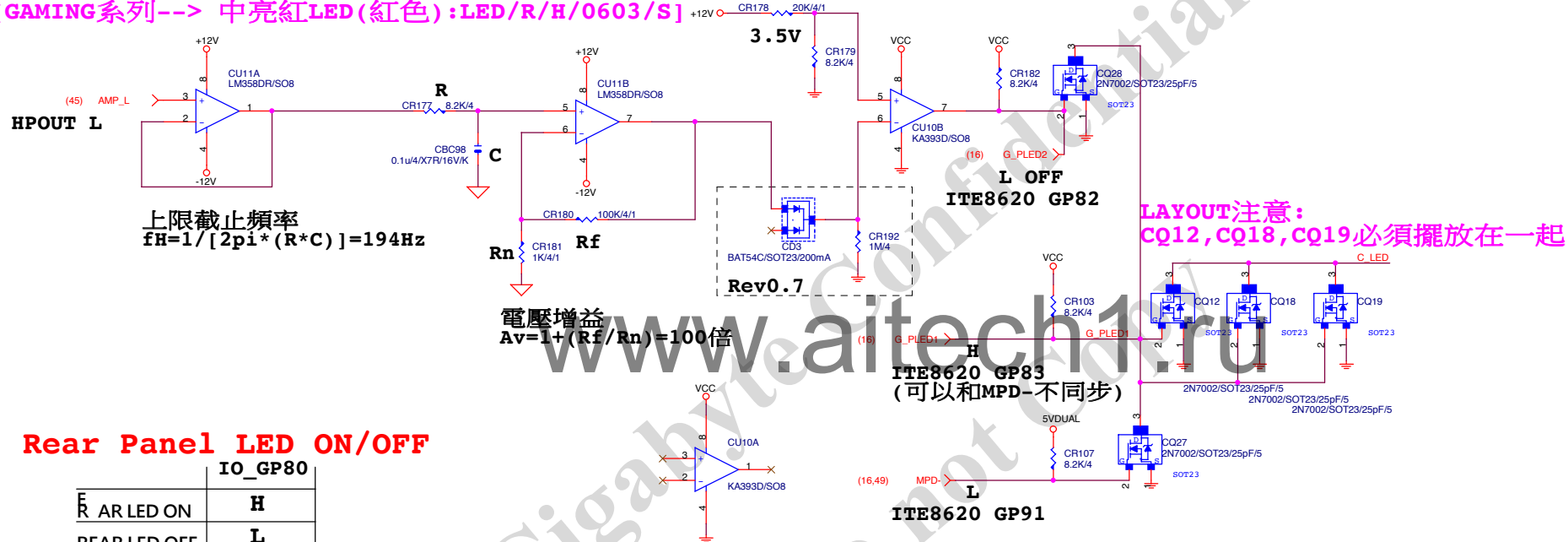


VALUE可變,LED顏色請自行修改

[UD系列--> 中亮黃LED(黃色):LED/Y/6/M/S]

[SOC系列--> 中亮橘LED(橘色):LED/O/M/0603/S]

[GAMING系列--> 中亮紅LED(紅色):LED/R/H/0603/S]



Rear Panel LED ON/OFF

	IO_GP80
REAR LED ON	H
REAR LED OFF	L

CLOSE TO AUDIO JACK

LAYOUT OPTION : SOC/UD7系列要LAYOUT,
其餘UD系列機種不留LAYOUT

AUDIO LED Control (沒有LPT model)

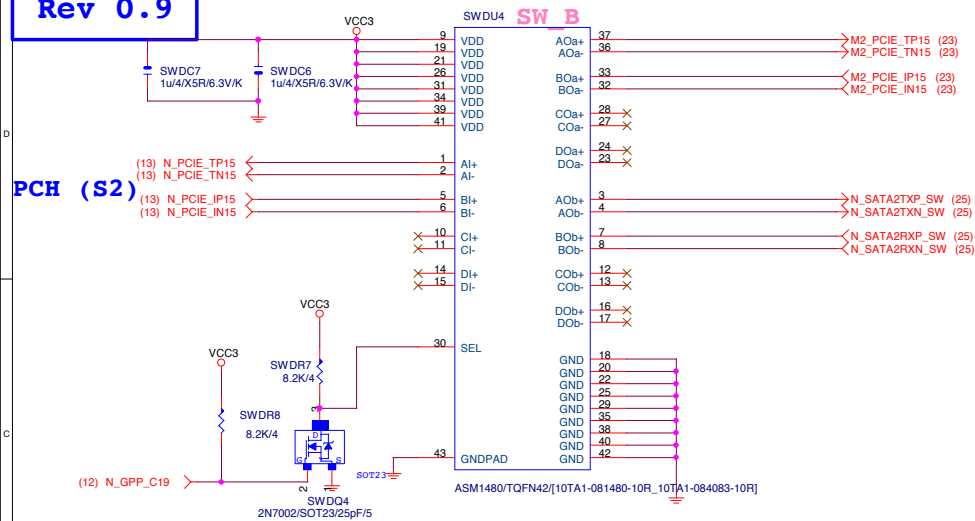
	IO GP82	IO GP83	IO GP91
Still Mode	L	H	L
OFF Mode	L	L	L
Pluse Mode	L	H	BREATH
Beat Mode	OD	H	L

AUDIO LED Control (有LPT model)

	IO GP92	IO GP17	IO GP91
Still Mode	L	H	L
OFF Mode	L	L	L
Pluse Mode	L	H	BREATH
Beat Mode	OD	H	L

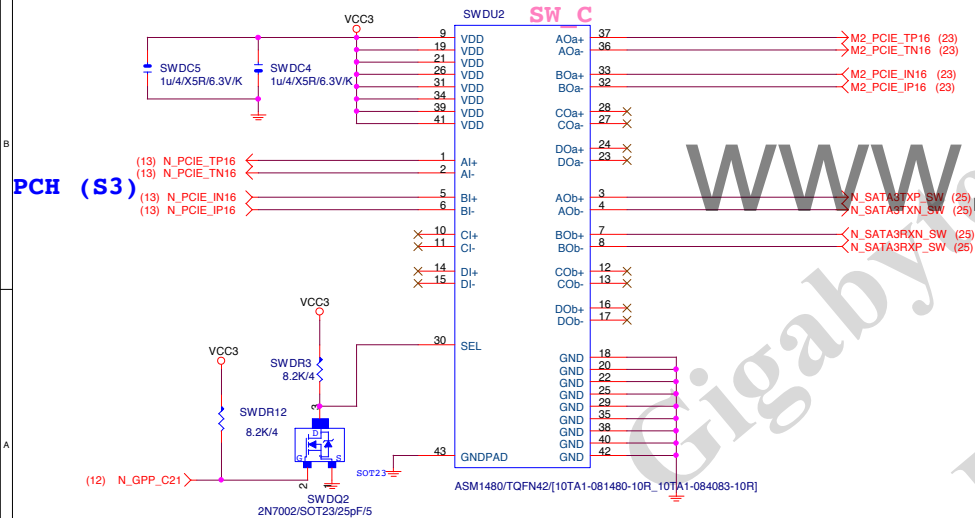
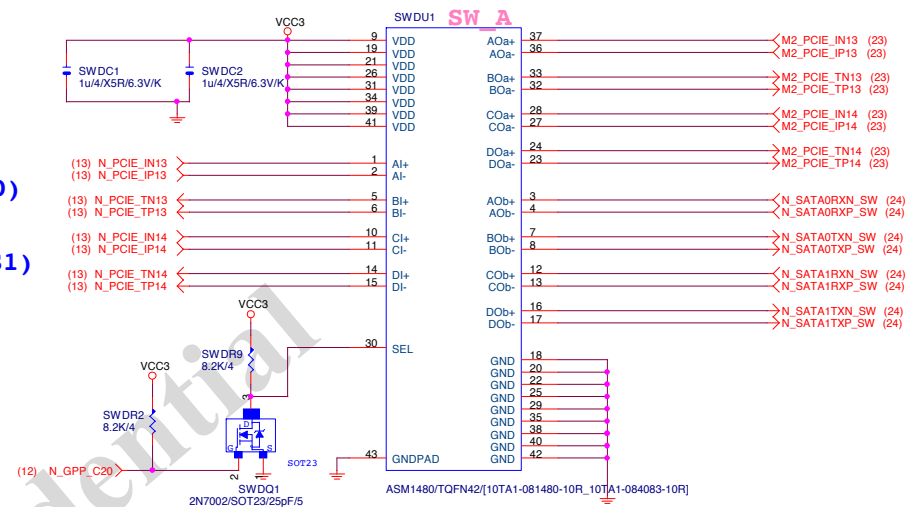
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PCH (S0)

PCH (S1)



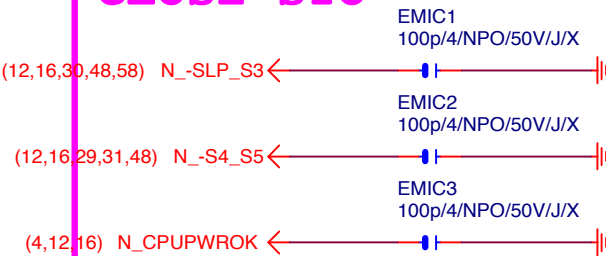
www.aitech1.ru

Gigabyte Technology
SWITCH

Title				
SWITCH				
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EMIC5, EMIC6, EMIC7 跟模組線路不同

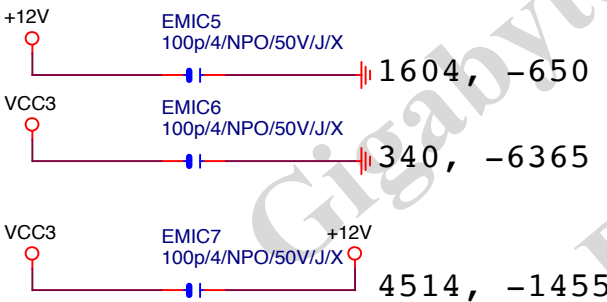
CLOSE SIO



CLOSE PCH



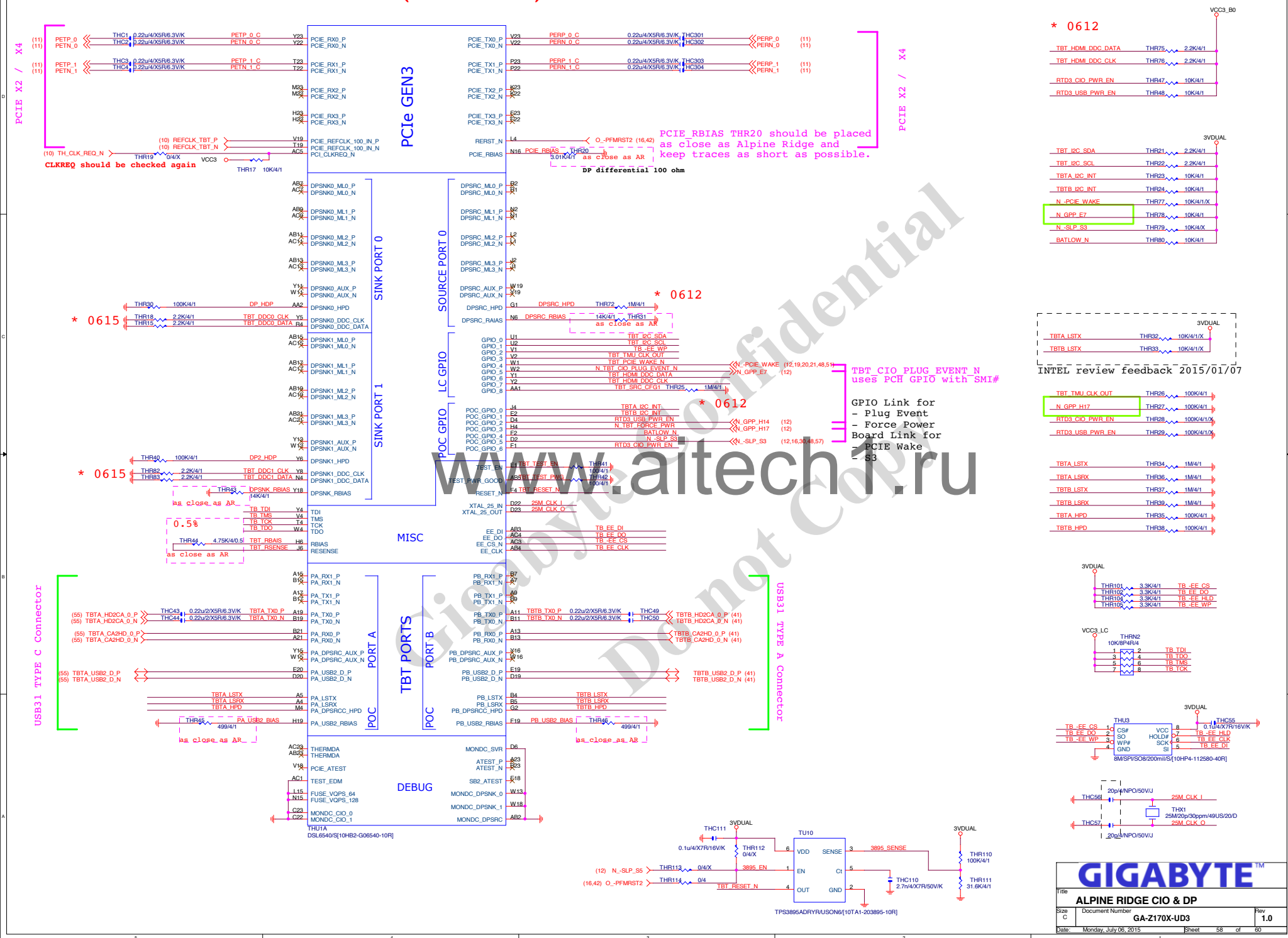
CLOSE AUDIO

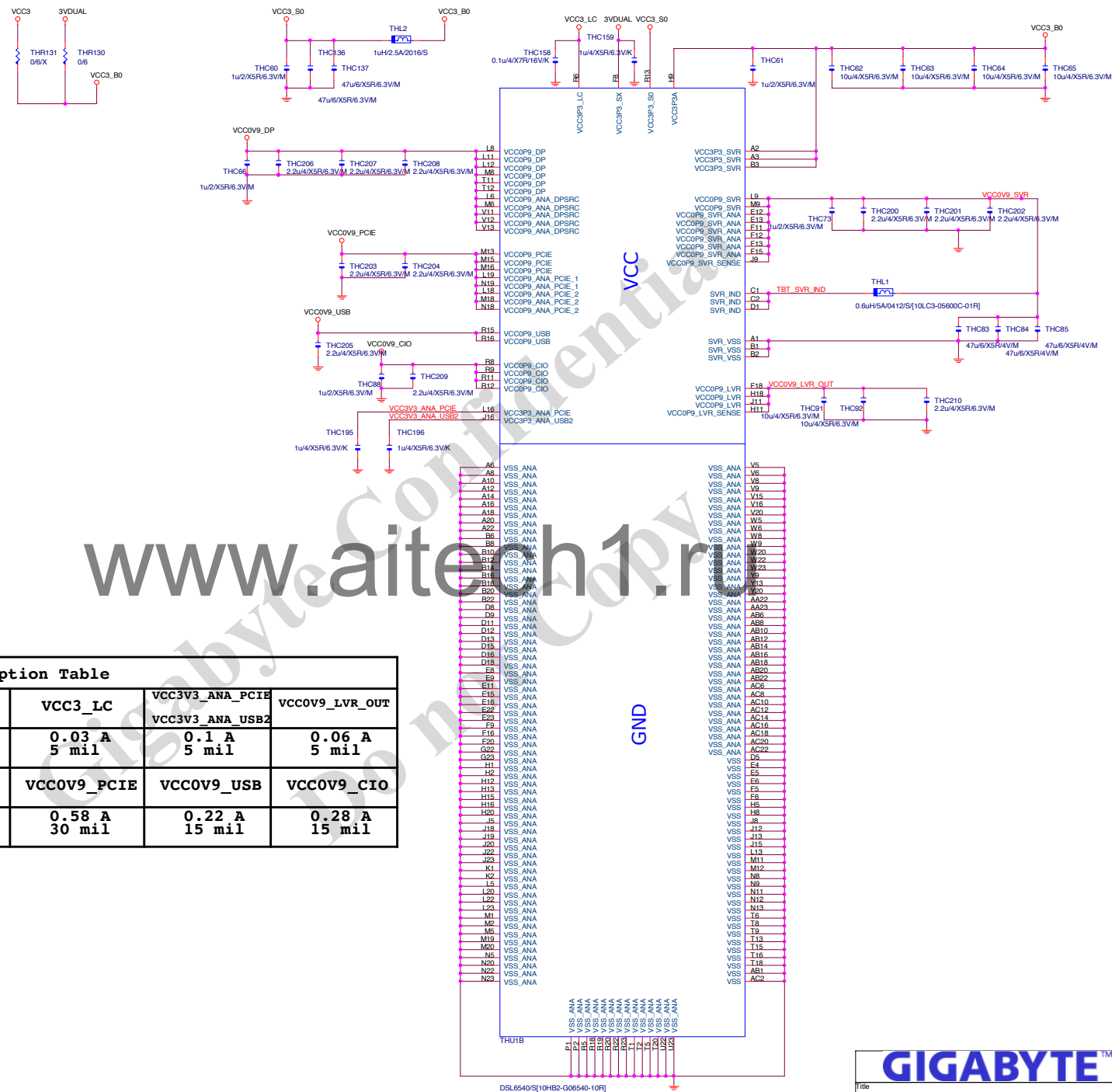


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Title			
EM/ESD			
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INTEL AR USB31 module SCH 0.61 (2015/06/15)





Power Consumption Table

Power Consumption Table					
	VCC3	3VDUAL	VCC3_LC	VCC3V3_ANA_PCIE VCC3V3_ANA_USB2	VCC0V9_LVR_OUT
Max Current(A)	1.05 A 40 mil	0.19 A 10 mil	0.03 A 5 mil	0.1 A 5 mil	0.06 A 5 mil
	VCC0V9_SVR	VCC0V9_DP	VCC0V9_PCIE	VCC0V9_USB	VCC0V9_CIO
Max Current(A)	1.83 A 80 mil	0.7 A 30 mil	0.58 A 30 mil	0.22 A 15 mil	0.28 A 15 mil

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ALPINE RIDGE POWER

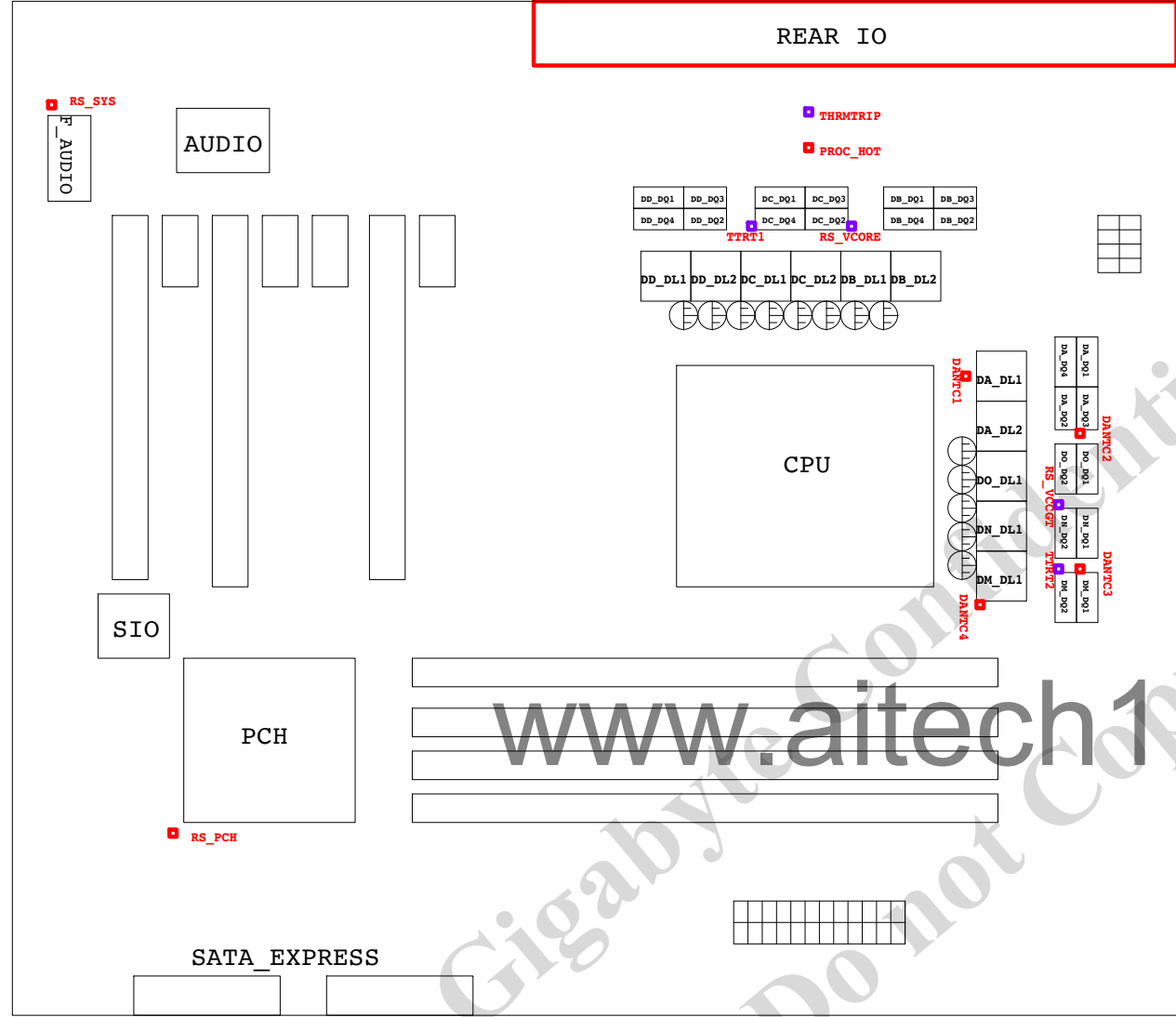
Document Number	
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熱敏電阻	擺放靠近位置	走線方式
DANTC1	DA_DL2	Differential
DANTC2	DA_DQ3	Differential
DANTC3	DM_DQ2	Differential
DANTC4	DM_DL1	Differential
RS_VCORE	DC_DQ4	N/A
RS_VCCGT	DM_DQ2	N/A
TTRT1	DC_DQ2	N/A
TTRT2	DN_DQ2	N/A
RS_PCH	PCH	N/A
RS_SYS	F_AUDIO	N/A